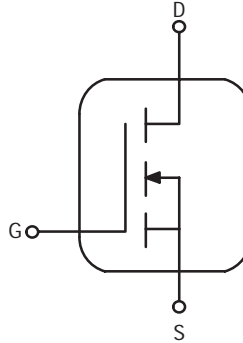


The RF MOSFET Line  
**RF Power Field Effect Transistors**  
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications at frequencies to 1.0 GHz. The high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 12.5 and 28 volt mobile, portable and base station equipment.

- Guaranteed Performance @ 945 MHz, 28 Volts  
Output Power = 7.5 Watts  
Power Gain = 15.5 dB  
Efficiency = 30%
- Capable of Handling 5:1 VSWR @ 28 Vdc, 945 MHz, 7.5 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- S-Parameter Characterization at High Bias Levels
- Suitable for 12.5 Volt Application
- Available in Tape and Reel. R1 Suffix = 500 Units per 12 mm, 7 inch Reel.
- LDMOS Models Available at <http://www.motorola.com/semiconductors/rf/models/>



**MRF181SR1**  
**MRF181ZR1**

**1.0 GHz, 7.5 W, 28 V**  
**LATERAL N-CHANNEL**  
**BROADBAND**  
**RF POWER MOSFETs**



**CASE 458B-02, STYLE 1**  
**(MRF181SR1)**



**CASE 458C-02, STYLE 1**  
**(MRF181ZR1)**

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 20$	Vdc
Drain Current — Continuous	$I_D$	2.0	Adc
Total Device Dissipation @ $T_C = 70^\circ\text{C}$ Derate above $70^\circ\text{C}$	$P_D$	36 0.278	Watts W/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.42	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

LIFETIME BUY

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LAST ORDER 31JUN04

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain–Source Breakdown Voltage ( $V_{GS} = 0, I_D = 50 \mu\text{Adc}$ )	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 28 \text{ Vdc}, V_{GS} = 0$ )	$I_{DSS1}$	—	—	1.0	$\mu\text{Adc}$
Zero Gate Voltage Drain Current ( $V_{DS} = 65 \text{ Vdc}, V_{GS} = 0$ )	$I_{DSS2}$	—	—	1.0	$\mu\text{Adc}$
Gate–Source Leakage Current ( $V_{GS} = 20 \text{ Vdc}, V_{DS} = 0$ )	$I_{GSS}$	—	—	1.0	$\mu\text{Adc}$

**ON CHARACTERISTICS**

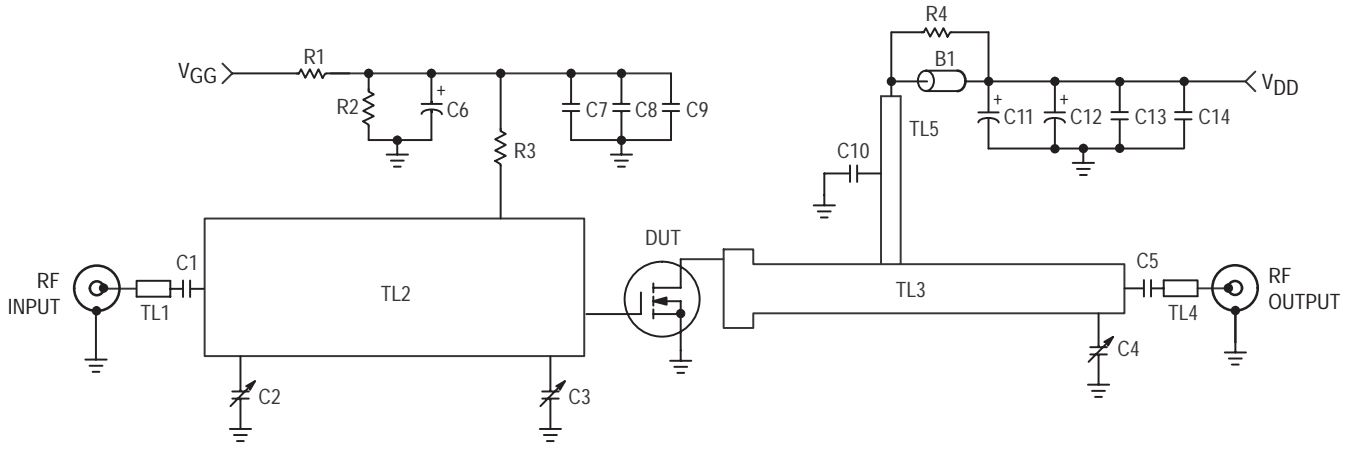
Gate Threshold Voltage ( $V_{DS} = 10 \text{ Vdc}, I_D = 55 \mu\text{Adc}$ )	$V_{GS(th)}$	2.0	3.6	4.0	Vdc
Drain–Source On–Voltage ( $V_{GS} = 10 \text{ Vdc}, I_D = 0.5 \text{ Adc}$ )	$V_{DS(on)}$	0.3	0.66	0.8	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28 \text{ Vdc}, I_D = 170 \text{ mAdc}$ )	$V_{GS(q)}$	3.5	—	5.5	Vdc

**DYNAMIC CHARACTERISTICS**

Input Capacitance ( $V_{DS} = 28 \text{ Vdc}, V_{GS} = 0, f = 1.0 \text{ MHz}$ )	$C_{iss}$	—	13	—	pF
Output Capacitance ( $V_{DS} = 28 \text{ Vdc}, V_{GS} = 0, f = 1.0 \text{ MHz}$ )	$C_{oss}$	—	6.6	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 28 \text{ Vdc}, V_{GS} = 0, f = 1.0 \text{ MHz}$ )	$C_{rss}$	—	0.69	—	pF

**FUNCTIONAL TESTS** (In Motorola Test Circuit. See Figure 1.)

Common–Source Power Gain ( $V_{DD} = 28 \text{ Vdc}, P_{out} = 7.5 \text{ W PEP}, I_{DQ} = 170 \text{ mA}, f_1 = 945 \text{ MHz}, f_2 = 945.1 \text{ MHz}, \text{Min } 15.5 \text{ dB}$ )	$G_{ps}$	15.5	17	—	dB
Drain Efficiency ( $V_{DD} = 28 \text{ Vdc}, P_{out} = 7.5 \text{ W PEP}, I_{DQ} = 170 \text{ mA}, f_1 = 945 \text{ MHz}, f_2 = 945.1 \text{ MHz}$ )	$\eta$	30	32.5	—	%
Input Return Loss ( $V_{DD} = 28 \text{ Vdc}, P_{out} = 7.5 \text{ W PEP}, I_{DQ} = 170 \text{ mA}, f_1 = 945 \text{ MHz}, f_2 = 945.1 \text{ MHz}$ )	IRL	—	–12.7	–9	dB
Intermodulation Distortion ( $V_{DD} = 28 \text{ Vdc}, P_{out} = 7.5 \text{ W PEP}, I_{DQ} = 170 \text{ mA}, f_1 = 945 \text{ MHz}, f_2 = 945.1 \text{ MHz}$ )	IMD	—	–30	–28.5	dBc
Output Mismatch Stress ( $V_{DD} = 28 \text{ Vdc}, P_{out} = 7.5 \text{ W CW}, I_{DQ} = 170 \text{ mA}, f_1 = 945 \text{ MHz}, \text{Load VSWR} = 5:1, \text{All Phase Angles}$ )	$\Psi$	No Degradation In Output Power			



B1	Short RF Bead, Fair Rite-2743019447	C10	30 pF Chip Capacitor, ATC 100B390CCA500X
C1	18 pF Chip Capacitor, ATC 100B180CCA500X	C11	250 $\mu$ F, 50 Vdc Electrolytic Capacitor, Mallory TC50025
C2, C3	0.8–8.0 pF Variable Capacitor, Johansen Gigatrim	N1, N2	Type N Connector
C4	0.4–2.5 pF Variable Capacitor, Johansen Gigatrim	R1	1.2 k $\Omega$ , 1/4 W Resistor
C5	100 pF Chip Capacitor, ATC 100A101CCA150X	R2	47 k $\Omega$ , 1/4 W Resistor
C6, C12	10 $\mu$ F, 50 Vdc Electrolytic Capacitor, Panasonic ECEV1HV100R	R3	10 k $\Omega$ , 1/4 W Chip Resistor
C7	43 pF Chip Capacitor, ATC 100B430CCA500X	R4	4.0 x 39 $\Omega$ , 1/8 W Chip Resistor
C8, C13	1000 pF Chip Capacitor, ATC 100B102CCA500X	TL1-TL5	Microstrip Line
C9, C14	0.1 $\mu$ F 50 Vdc Ceramic, Kemet CDR33BX104AKWS	Ckt Board	1/32" Glass Teflon <sup>®</sup> , $\epsilon_r = 2.55$ , Arlon-GX-0300-55-22

Figure 1. MRF181 Test Circuit Schematic

## TYPICAL CHARACTERISTICS

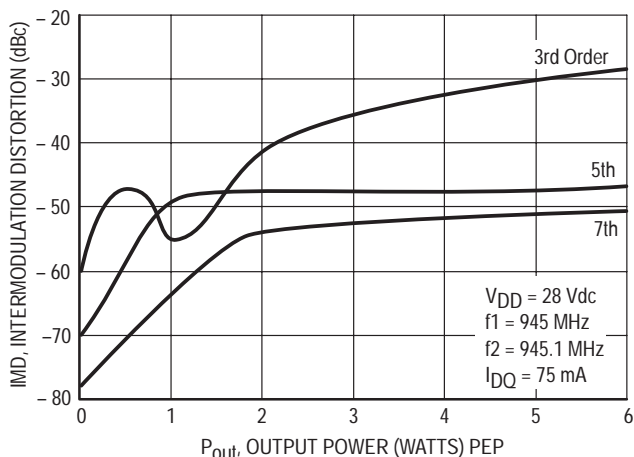


Figure 2. Intermodulation Distortion Products versus Output Power

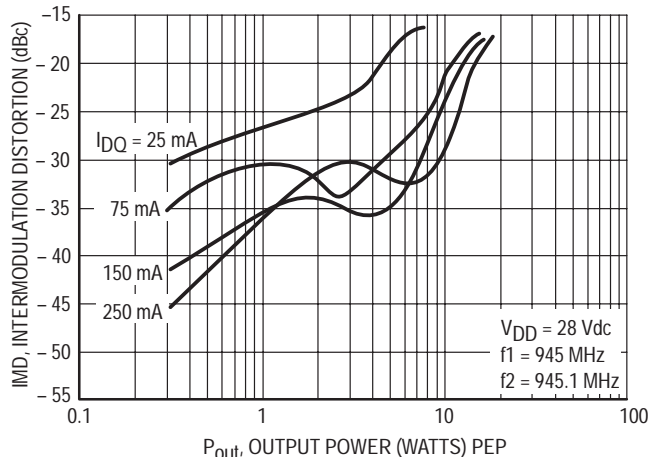


Figure 3. Intermodulation Distortion versus Output Power

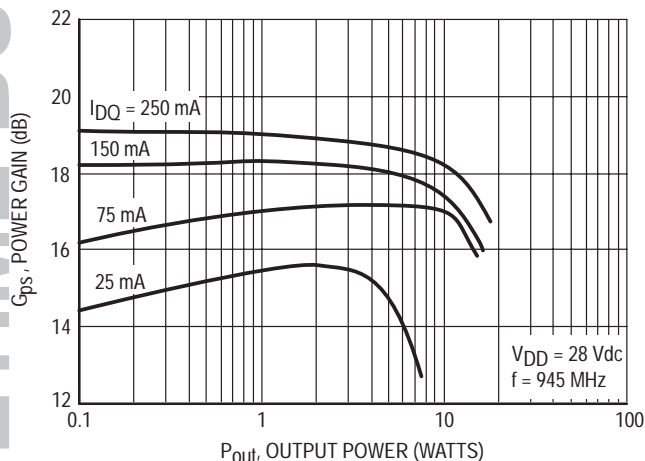


Figure 4. Power Gain versus Output Power

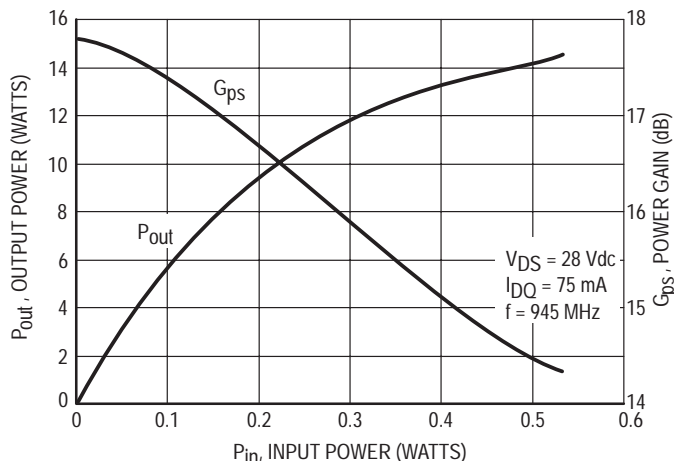


Figure 5. Output Power versus Input Power

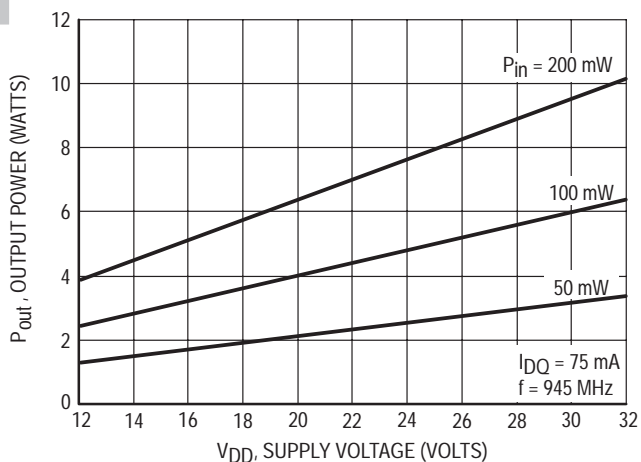


Figure 6. Output Power versus Supply Voltage

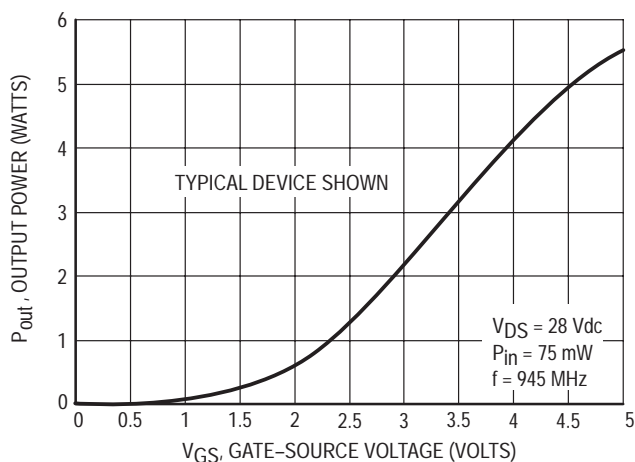


Figure 7. Output Power versus Gate Voltage

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### TYPICAL CHARACTERISTICS

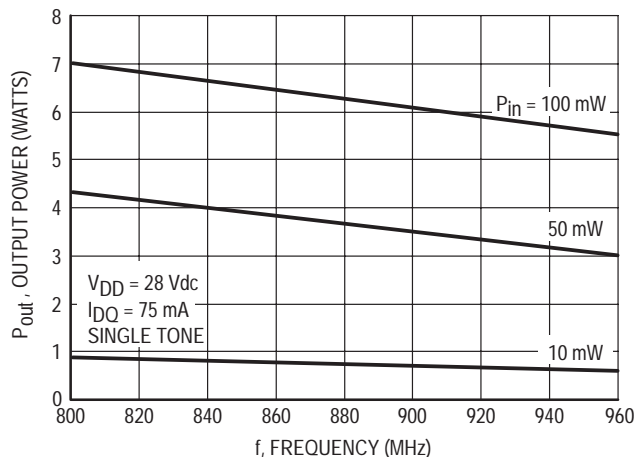


Figure 8. Output Power versus Frequency

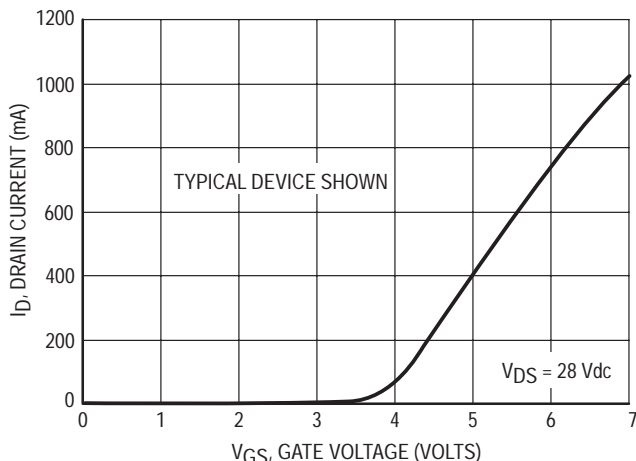


Figure 9. Drain Current versus Gate Voltage

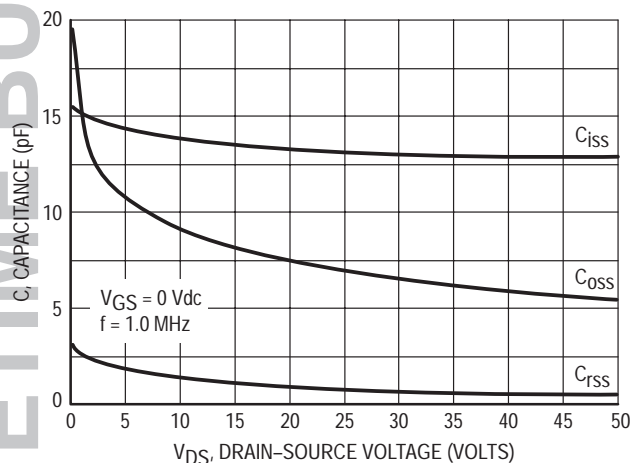


Figure 10. Capacitance versus Voltage

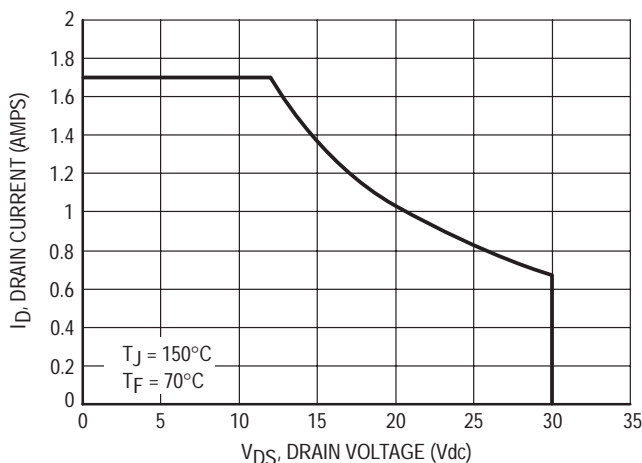


Figure 11. DC Safe Operating Area

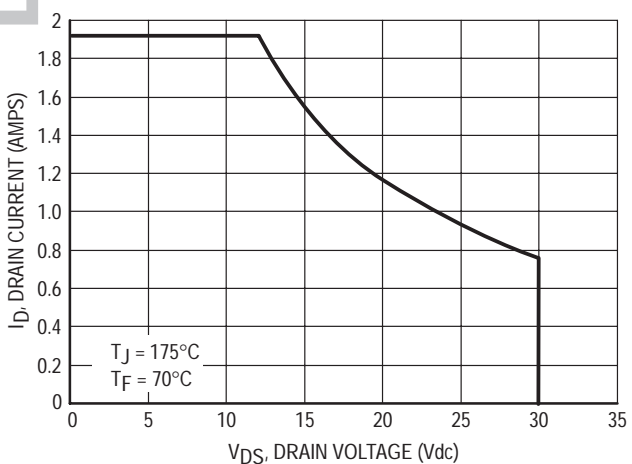


Figure 12. DC Safe Operating Area

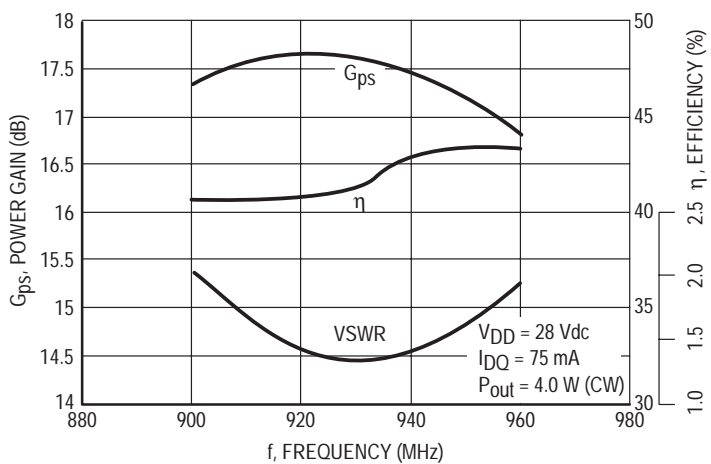


Figure 13. Performance in Broadband Circuit

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TYPICAL CHARACTERISTICS

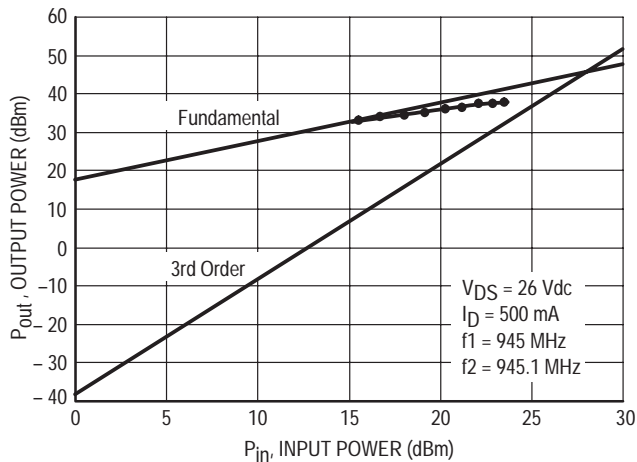


Figure 14. Class A Third Order Intercept Point

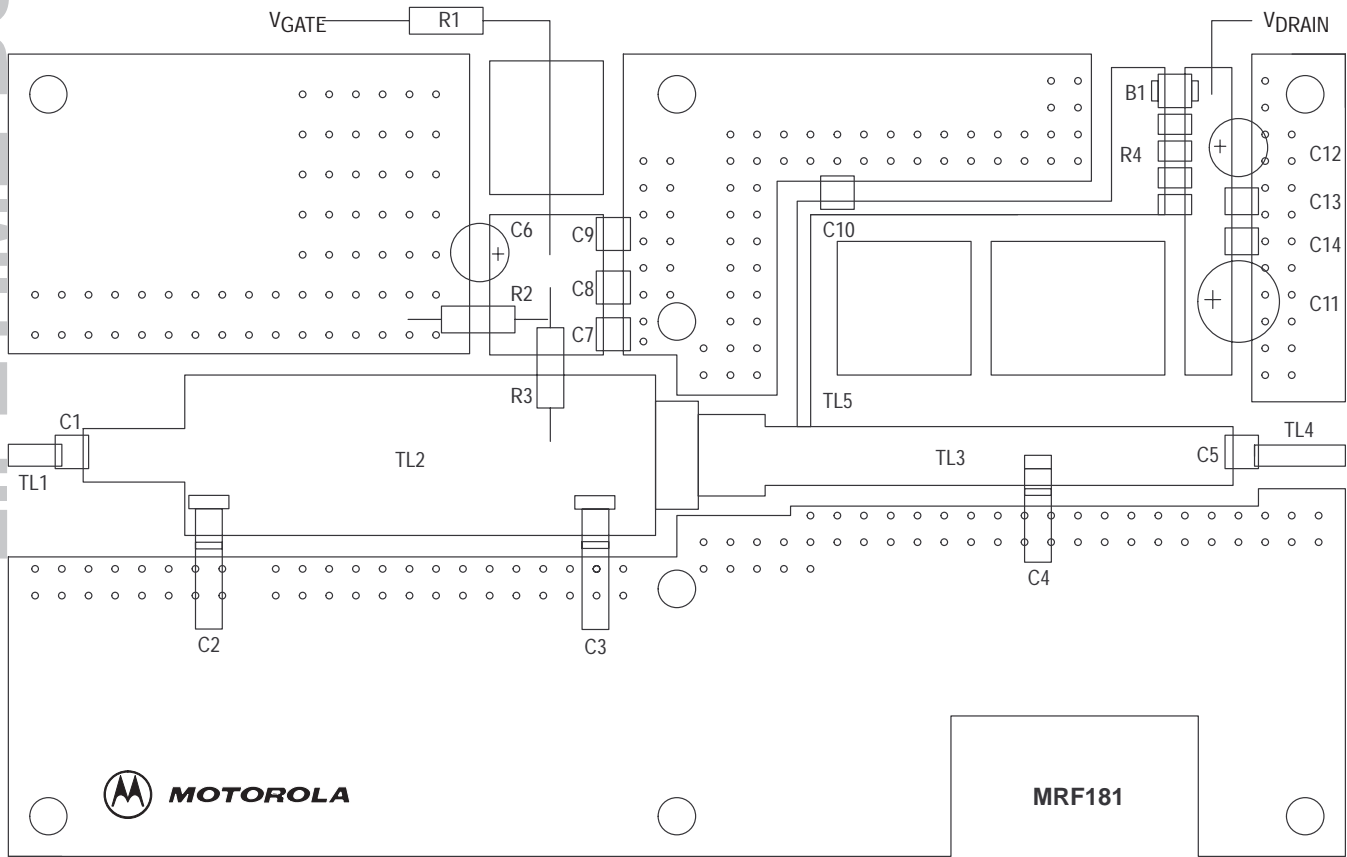
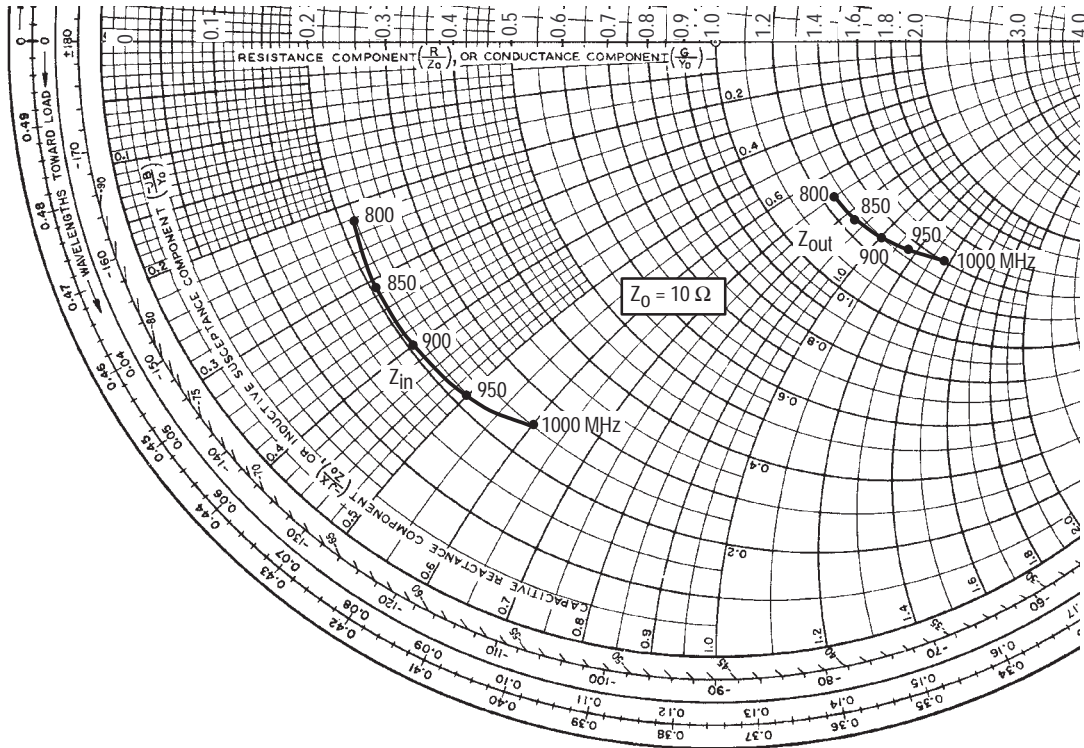


Figure 15. Component Parts Layout

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$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 170 \text{ mA}$ ,  $P_{out} = 7.5 \text{ W (PEP)}$

f MHz	$Z_{in}$ Ohms	$Z_{OL}^*$ Ohms
800	$2.15 - j2.2$	$12.45 - j7.0$
850	$2.11 - j3.5$	$12.65 - j8.5$
900	$2.14 - j4.0$	$12.95 - j10.0$
950	$2.20 - j5.0$	$13.52 - j11.5$
1000	$2.35 - j5.8$	$14.11 - j13.7$

$Z_{in}$  = Complex conjugate of source impedance.  
 $Z_{OL}^*$  = Complex conjugate of the load impedance at given output power, voltage, frequency and efficiency.

Note:  $Z_{OL}^*$  was chosen based on tradeoffs between gain, drain efficiency, and device stability.

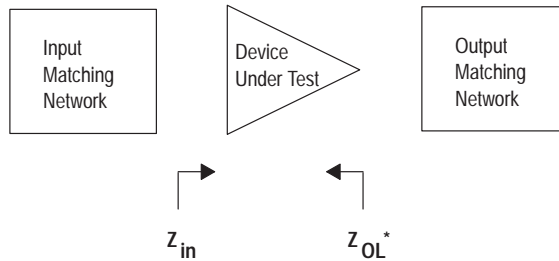


Figure 16. Series Equivalent Input and Output Impedance

Table 1. Common Emitter S-Parameters ( $V_{DS} = 26 \text{ Vdc}$ )

$I_D = 500 \text{ mA}$

f MHz	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>	∠φ
10	0.944	-10	31.66	174	0.004	84	0.772	-7
20	0.940	-20	31.23	168	0.008	78	0.765	-14
30	0.934	-30	30.54	162	0.011	73	0.752	-21
40	0.927	-39	29.66	156	0.015	67	0.736	-28
50	0.918	-48	28.62	151	0.018	62	0.718	-34
100	0.873	-83	22.81	129	0.028	41	0.620	-60
150	0.843	-106	17.94	114	0.033	28	0.549	-78
200	0.827	-121	14.44	103	0.035	18	0.509	-90
250	0.820	-131	11.94	95	0.036	11	0.490	-99
300	0.817	-139	10.09	88	0.036	6	0.484	-105
350	0.817	-145	8.69	82	0.036	1	0.487	-111
400	0.820	-149	7.59	77	0.035	-3	0.496	-115
450	0.823	-153	6.71	72	0.034	-7	0.508	-118
500	0.828	-156	5.99	68	0.033	-10	0.523	-122
550	0.833	-159	5.39	64	0.032	-12	0.538	-125
600	0.839	-161	4.88	60	0.031	-15	0.555	-127
650	0.845	-163	4.44	56	0.029	-17	0.572	-130
700	0.851	-165	4.06	52	0.028	-19	0.589	-132
750	0.857	-167	3.73	49	0.026	-20	0.606	-134
800	0.864	-169	3.44	45	0.025	-22	0.622	-137
850	0.870	-171	3.18	42	0.023	-23	0.638	-139
900	0.876	-172	2.95	39	0.022	-23	0.654	-141
950	0.882	-174	2.74	36	0.020	-24	0.669	-143
1000	0.888	-175	2.55	33	0.018	-24	0.683	-144
1050	0.893	-176	2.38	30	0.017	-23	0.697	-146
1100	0.899	-178	2.23	28	0.015	-22	0.710	-148
1150	0.904	-179	2.09	25	0.014	-20	0.722	-150
1200	0.909	180	1.96	22	0.012	-16	0.734	-151
1250	0.914	179	1.85	20	0.011	-12	0.745	-153
1300	0.918	177	1.74	17	0.010	-6	0.756	-155
1350	0.922	176	1.64	15	0.009	1	0.766	-156
1400	0.927	175	1.55	13	0.009	10	0.775	-158
1450	0.931	174	1.47	10	0.008	20	0.784	-159
1500	0.934	173	1.39	8	0.008	30	0.793	-161

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# NOTES

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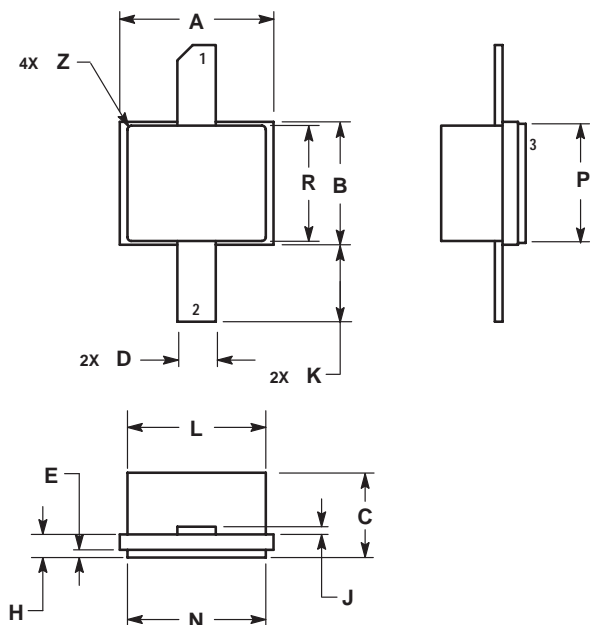
LAST ORDER 31JUN04 LAST SHIP 31JAN05

# NOTES

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PACKAGE DIMENSIONS

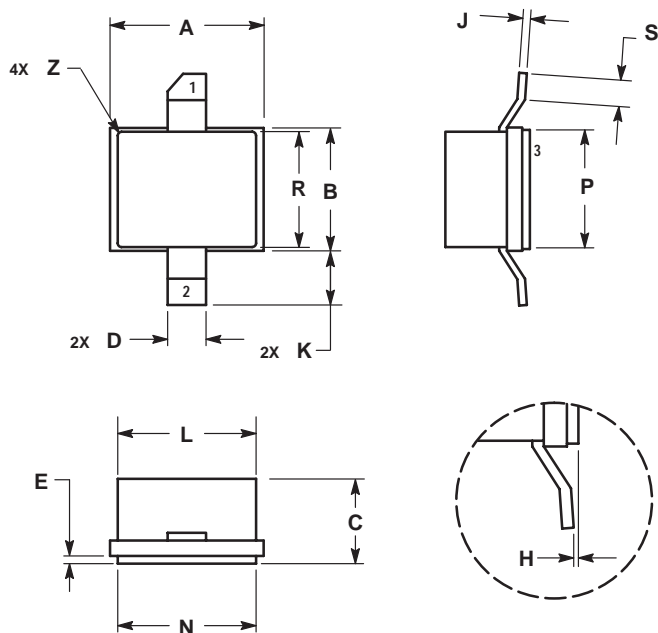


- NOTES:
1. CONTROLLING DIMENSIONS: INCHES.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. ALL DIMENSIONS ARE SYMMETRICAL ABOUT CENTERLINE UNLESS OTHERWISE NOTED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.197	0.203	5.004	5.156
B	0.157	0.163	3.988	4.140
C	0.085	0.110	2.159	2.794
D	0.047	0.053	1.194	1.346
E	0.004	0.010	0.102	0.254
H	0.025	0.031	0.635	0.787
J	0.004	0.010	0.102	0.254
K	0.060	0.110	1.524	2.794
L	0.177	0.183	4.496	4.648
N	0.180	0.200	4.572	5.080
P	0.140	0.160	3.556	4.064
R	0.147	0.153	3.734	3.886
Z	---	0.020	---	0.508

- STYLE 1:  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE

CASE 458B-02  
 ISSUE C  
 (MRF181SR1)



- NOTES:
1. CONTROLLING DIMENSIONS: INCHES.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSION H (PACKAGE COPLANARITY): THE BOTTOM OF LEADS AND REFERENCE PLANE T MUST BE COPLANAR WITHIN DIMENSION H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.197	0.203	5.004	5.156
B	0.157	0.163	3.988	4.140
C	0.085	0.110	2.159	2.794
D	0.047	0.053	1.194	1.346
E	0.004	0.010	0.102	0.254
H	0.000	0.004	0.000	0.102
J	0.004	0.010	0.102	0.254
K	0.050	0.090	1.270	2.286
L	0.177	0.183	4.496	4.648
N	0.180	0.200	4.572	5.080
P	0.140	0.160	3.556	4.064
R	0.147	0.153	3.734	3.886
Z	---	0.020	---	0.508

- STYLE 1:  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE


CASE 458C-02  
 ISSUE C  
 (MRF181ZR1)

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