NOTE: The theory in this application note is still applicable, but some of the products referenced may be discontinued.

60 Watts, GSM 900 MHz, LDMOS Two-Stage Amplifier

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INTRODUCTION

This application note demonstrates the feasibility of a complete RF amplifier using Freescale LDMOS transistors in Class AB. The complete design requires standard piece parts and components only yet exhibits superior performance in terms of gain, efficiency, power and ruggedness in a GSM 900 MHz base station environment.

DESIGN RULES AND GOALS

The goal of the design is to provide an RF amplifier for GSM 900 MHz base stations. The amplifier has to deliver an output power of 60 Watts CW (continuous wave) with an efficiency as high as possible, and a gain in the range of 30 dB. The final transistor chosen is the MRF184, a second generation LDMOS transistor from Freescale. The MRF184 is able to deliver 60 W with more than 10 dB gain in a linear configuration. The power supply is 26 V (typically 24 to 28 V for base stations). The driver stage has to deliver a maximum power in the range of 4 W, but in order to have very good linearity (concentrating the non-linearities in the final stage increases the overall efficiency) the MRF6522-10, a 10 W SMD transistor was chosen. This device is also a second generation LDMOS transistor from Freescale. Matching networks are done on an epoxy substrate (GI180 from POLYCLAD, ε_r = 4.0), and the PCB is screwed on the base plate using standard 2.5 mm screws. SMD 0805 components are used, and the "ACCUP" series from AVX are used for "high Q" capacitors. All metalized holes in the PCB have a 0.5 mm diameter, including the hole area used for the grounding and the cooling of the driver.

IMPEDANCE MEASUREMENTS

The first step in such a design is the determination of the source and load impedances for the transistors, optimized for best performances in a GSM application. The source and load impedance values are provided in Table 1. Note that values are quite different from the "S" parameters for the MRF184 and MRF6522-10. "S" parameters should not be used for the design of a high power Class AB amplifier and are only suitable as a starting point to verify maximum available gain and stability over a specified bandwidth.

It can be seen in the Smith® chart for Figure 1 that the impedances of the two devices are not very dispersed, which means that it will be quite easy to build a wideband amplifier. This will allow mass production of the amplifier with no or very limited tuning.

Smith is a registered trademark of Analog Instruments Co.
Libra is a trademark of Hewlett-Packard, Inc.

freescale™ semiconductor

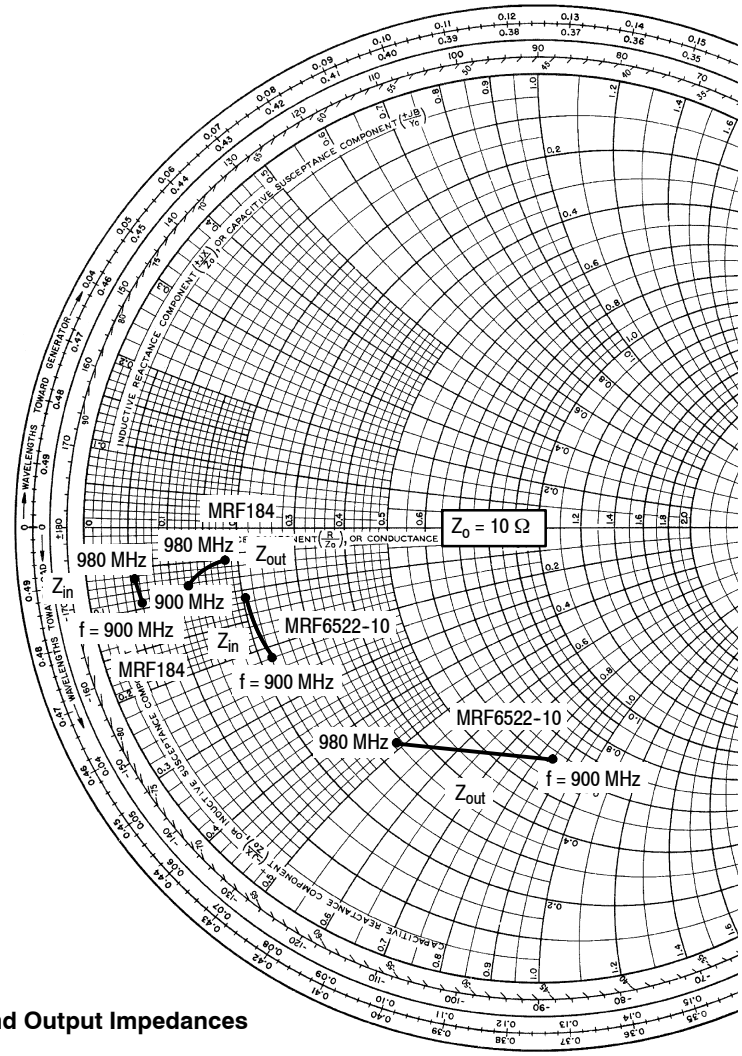


Figure 1. Input and Output Impedances

Table 1. Input and Output Impedances

MRF184 (26 V, 70 Watts)

f MHz	S_{11}	S_{22}	Z_{in} Ohms	Z_{out} Ohms
900	0.66 + j4.71	2.41 + j2.91	0.60 – j0.93	1.48 – j0.82
920	0.64 + j4.79	2.32 + j2.94	0.59 – j0.88	1.50 – j0.77
940	0.61 + j4.89	2.26 + j3.02	0.57 – j0.82	1.62 – j0.71
960	0.58 + j4.97	2.23 + j3.05	0.56 – j0.73	1.79 – j0.60
980	0.59 + j5.03	2.22 + j3.27	0.55 – j0.66	1.82 – j0.49

MRF6522-10 (26 V, 12 Watts)

f MHz	S_{11}	S_{22}	Z_{in} Ohms	Z_{out} Ohms
900	2.65 – j2.44	7.08 – j9.21	2.20 – j2.20	6.05 – j8.50
920	2.55 – j2.25	6.85 – j8.96	2.18 – j1.89	5.76 – j8.09
940	2.60 – j1.99	6.66 – j8.78	2.14 – j1.77	4.88 – j7.15
960	2.47 – j1.81	6.52 – j8.51	2.10 – j1.65	4.53 – j6.36
980	2.44 – j1.58	6.32 – j8.29	2.05 – j1.32	3.54 – j4.97

FINAL STAGE DESIGN

Although the critical task in a multistage amplifier design is the interstage matching, it is recommended to focus on the final stage matching (50 Ω input, 50 Ω output) as a starting point. The above impedances have been used in a simulator (Libra™ from HP-EEsof) to define the input and output matching networks. The results are shown in Figure 2. At the output, some capacitors have been split in two in order to avoid heating problems in the component itself. It can be seen that the matching networks are quite simple and use standard values of components.

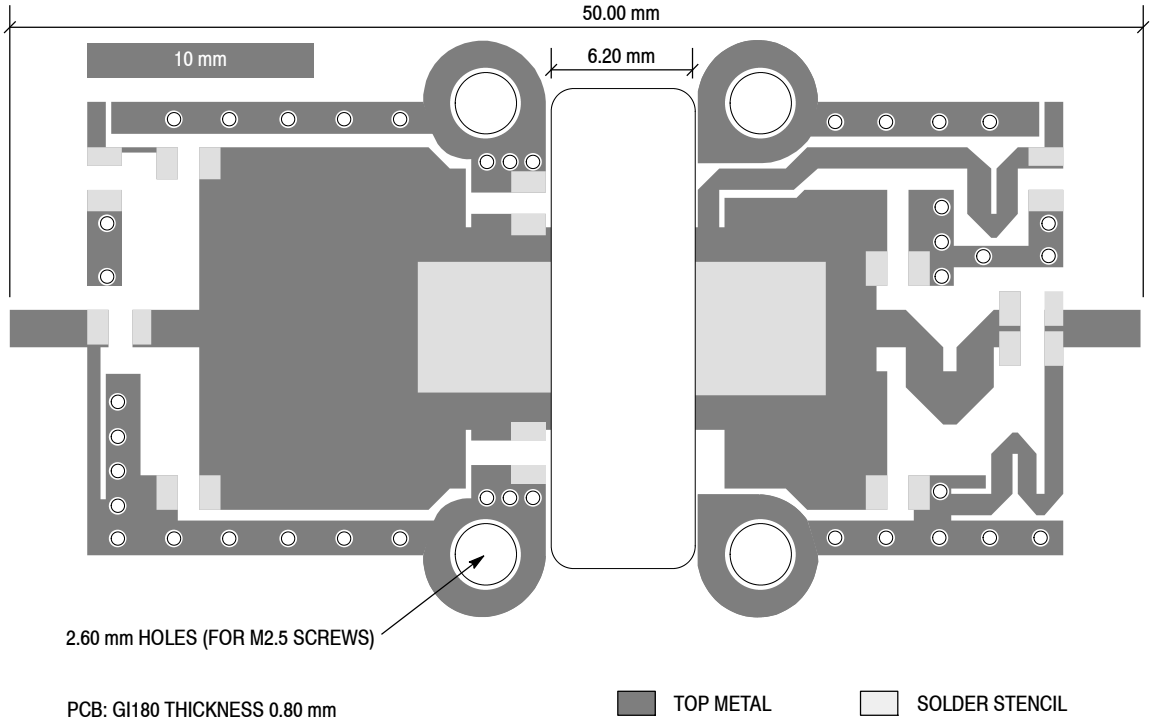
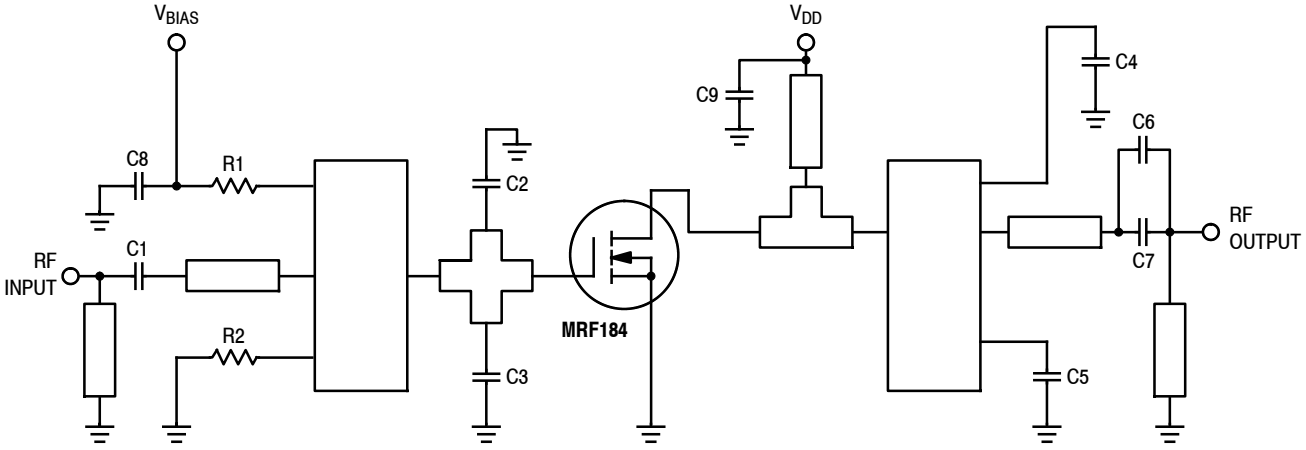


Figure 2. Final Stage PCB



C1	5.6 pF (AVX ACCUP)	C7	2.2 pF (AVX ACCUP)
C2, C3	15 pF (AVX ACCUP)	C8, C9	470 pF (NPO)
C4, C5	10 pF (AVX ACCUP)	R1	3.9 kΩ
C6	2.7 pF (AVX ACCUP)	R2	1 kΩ

Figure 3. Final Stage Electrical Schematic

Figure 2 shows a view of the PCB with the positioning of the components (solder stencil). A fine tuning of the amplifier can be done in a specific application by adjusting the length of the parallel inductances (0.5 mm printed lines). In Figure 4, one can see the complete amplifier board including bias circuit. A solder mask has been added on the PCB in order to ensure good positioning of the RF components. The amplifier was constructed with only a resistor bridge, since the purpose of this paper was not to concentrate on the different types of bias circuits. Of course, any type of bias circuit can be implemented with the same RF circuit, thermally compensated or not.

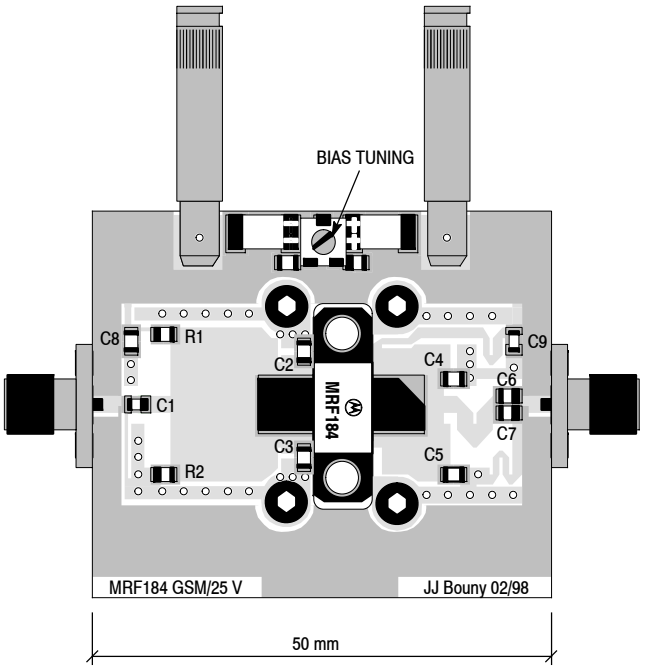


Figure 4. Final Stage Complete Amplifier

FINAL STAGE MEASUREMENTS

A complete set of measurements was taken on the final stage. Figures 5 to 8 show measurements taken with a network analyzer.

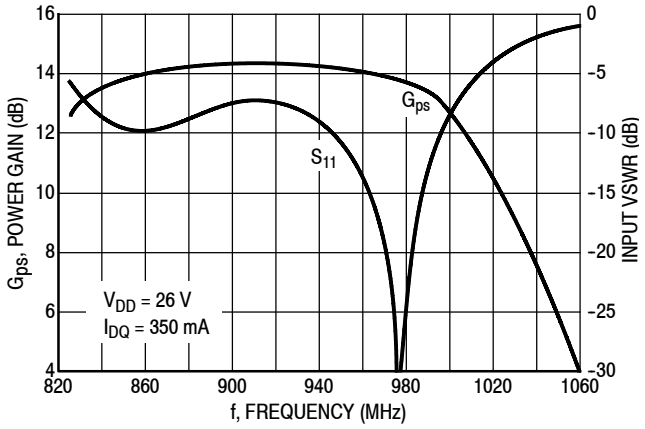


Figure 5. Power Gain, S_{11} = f (Frequency)

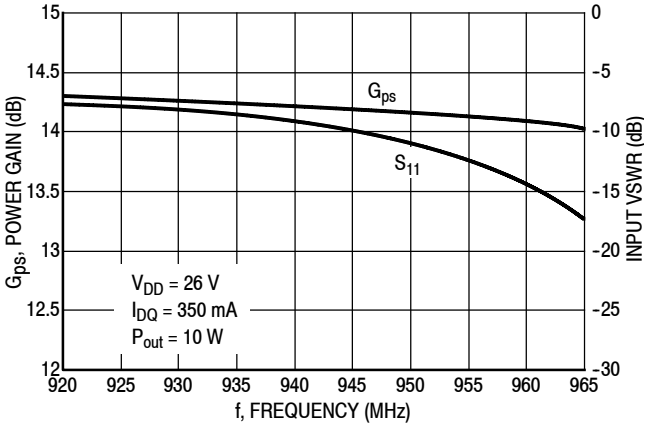


Figure 6. Power Gain, S_{11} = f (Frequency)

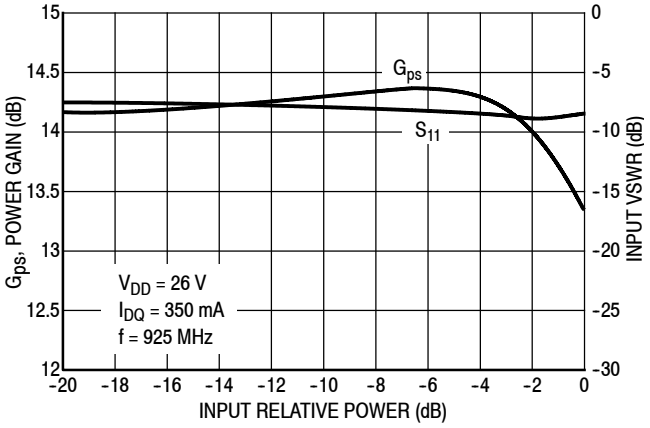


Figure 7. Power Gain, S_{11} = f (P_{in} @ 925 MHz)

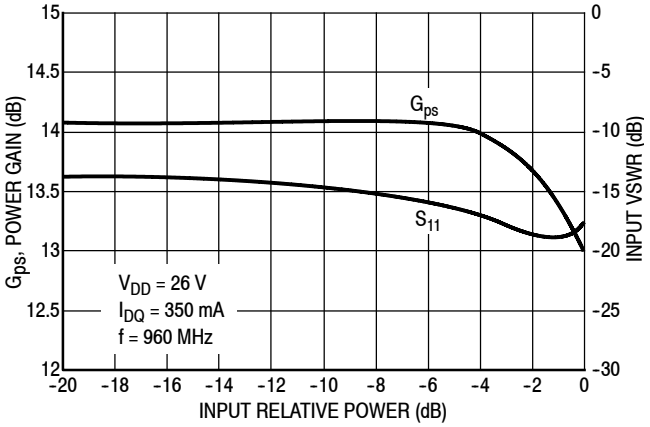


Figure 8. Power Gain, S_{11} = f (P_{in} @ 960 MHz)

Figures 5 and 6 show gain and input return losses versus frequency (GSM band and wide band), and Figures 7 and 8 show gain and input return losses versus input power at both ends of the band (up to 1 dB compression point). Input power scale is relative to the input power necessary to have 1 dB gain compression.

At 1 dB compression point, the following results are obtained:

925 MHz / 26 V / 35°C base−plate
66 W / **13.2 dB** gain / **58.6%** drain efficiency

960 MHz / 26 V / 35°C base−plate
64 W / **13.1 dB** gain / **55.6%** drain efficiency

As shown in Figures 9 to 11, some additional measurements have also been done to show the behavior of the amplifier versus temperature, power supply and saturation level.

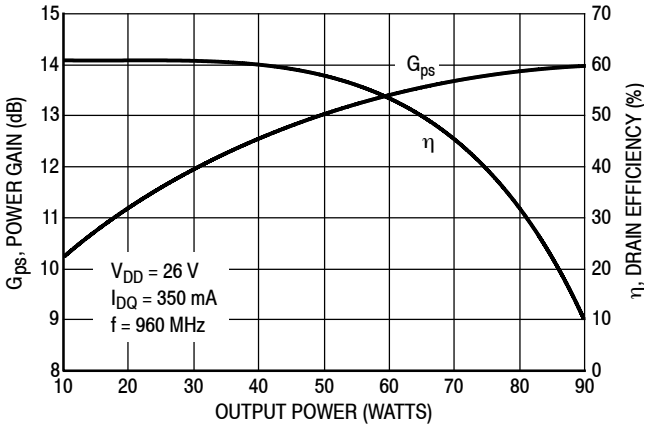


Figure 9. Power Gain, Efficiency = f (P_{out})

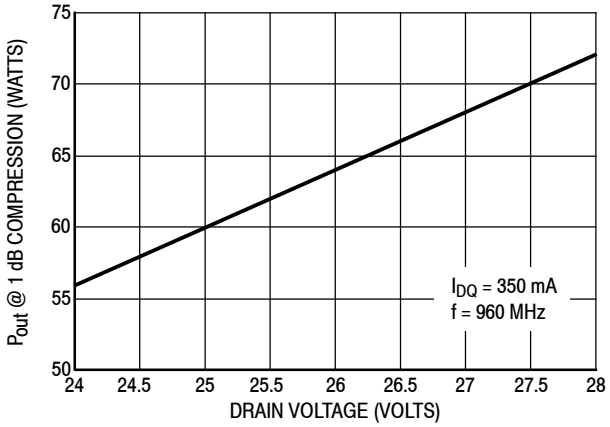


Figure 10. P_{out} @ 1 dB Compression = f (V_{DD})

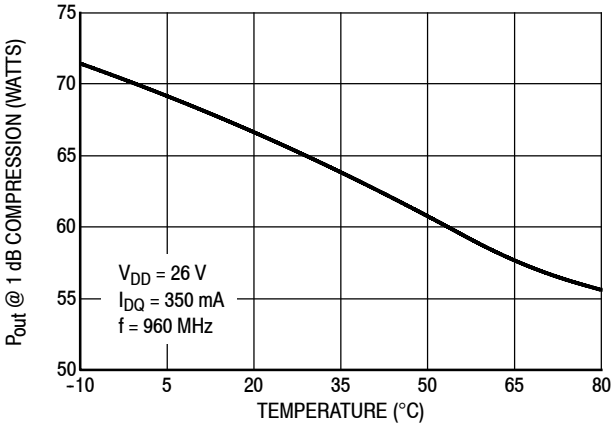


Figure 11. P_{out} @ 1 dB Compression = f (Temperature)

As seen in Figure 12, reverse intermodulation has also been measured with two different levels of spurious in order to cover most of the applications. Spacing between the main tone and the spurious is 400 kHz, and reverse intermodulation is measured by reference to the level of the main carrier.

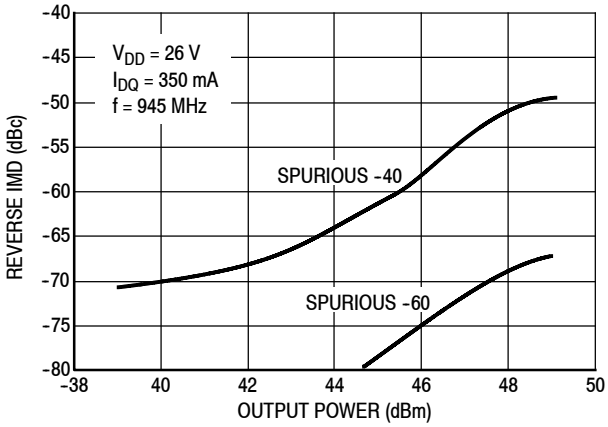


Figure 12. Reverse IMD = f (P_{out})

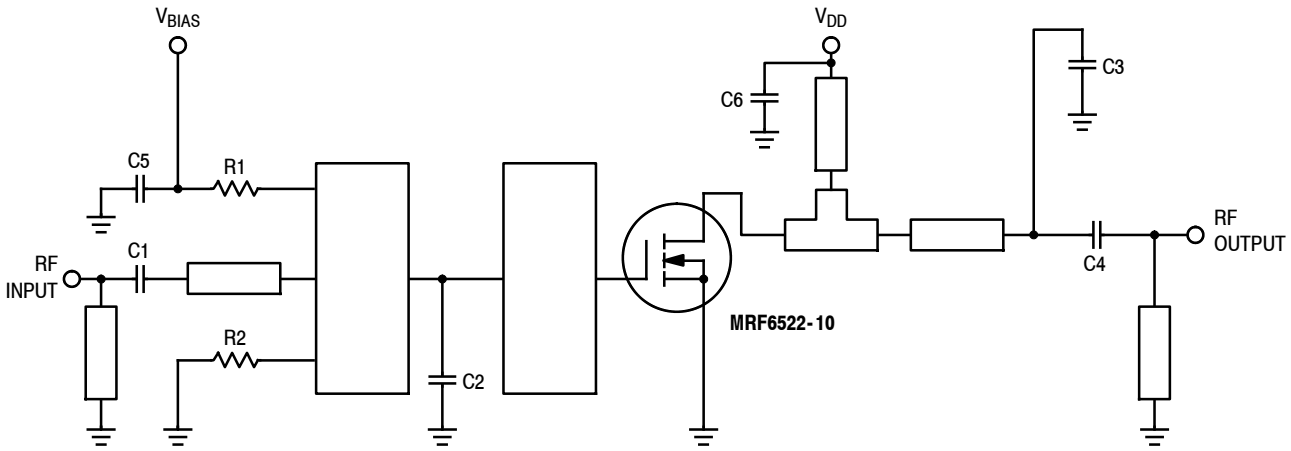
DRIVER STAGE DESIGN

The driver stage was also matched as a “stand alone” in order to assess what the performance would be as the final stage of a microcell (low power) base station. Figures 13 to 15 show the design of the amplifier, and Figures 16 and 17 show the results obtained versus frequency.

At 1 dB compression, the following results are obtained:

925 MHz / 26 V / 35°C base-plate
15 W / **18.5 dB** gain / **62%** efficiency

960 MHz / 26 V / 35°C base-plate
12 W / **18.0 dB** gain / **57%** efficiency



C1	8.2 pF (AVX ACCUP)	C5, C6	470 pF (NPO)
C2	18 pF (AVX ACCUP)	R1	3.9 kΩ
C3	10 pF (AVX ACCUP)	R2	1 kΩ
C4	12 pF (AVX ACCUP)		

Figure 13. Driver Stage Electrical Schematic

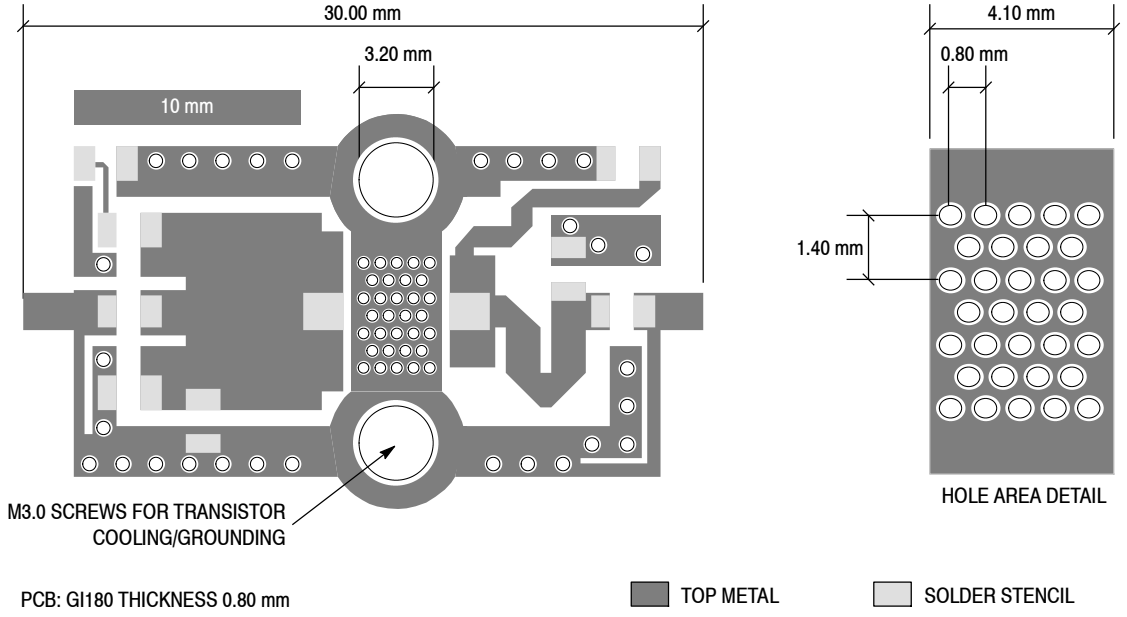


Figure 14. Driver Stage PCB

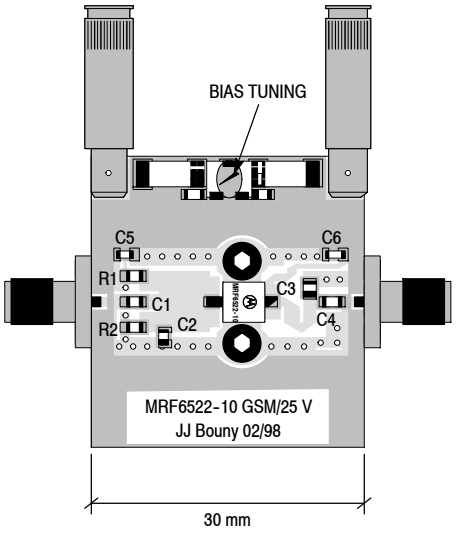


Figure 15. Driver Stage Complete Amplifier

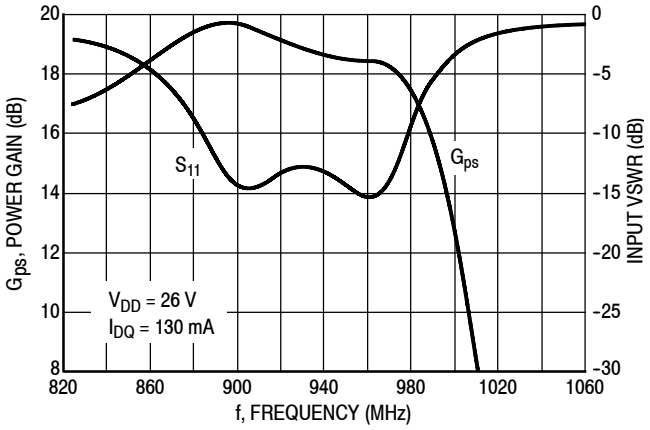


Figure 16. Power Gain, S_{11} = f (Frequency)

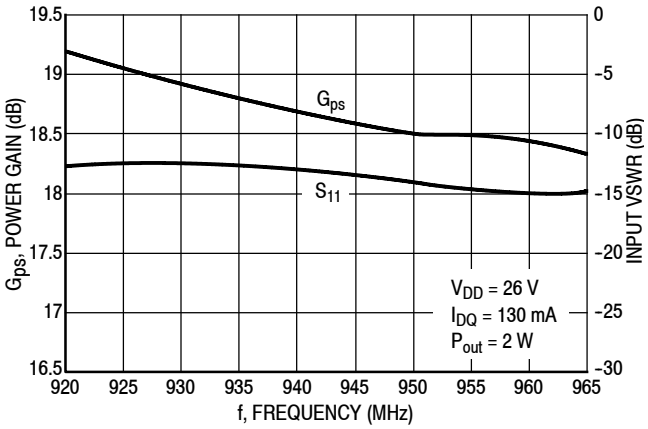
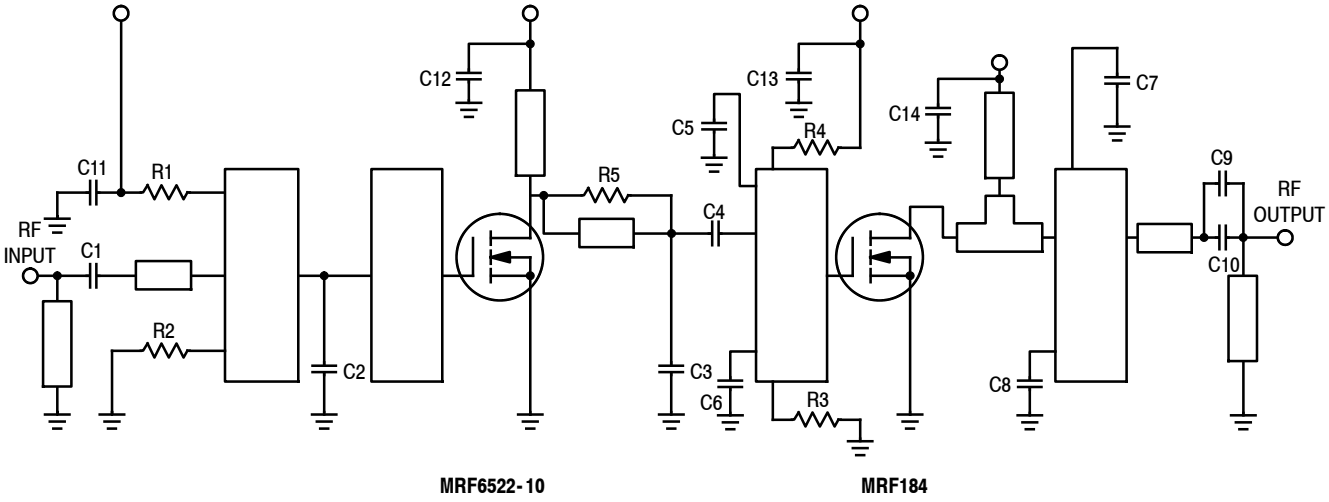


Figure 17. Power Gain, S_{11} = f (Frequency)

As seen in Figure 16, the driver stage and the final stage have a bandwidth much larger than the GSM band (925 MHz–960 MHz), and could also be used for the DAMPS 900.

TWO–STAGE DESIGN

For the design of the two–stage amplifier, the output matching network of the final stage and the input matching network of the driver stage are used. An interstage network will then be designed that goes directly from the output impedance of the driver to the input impedance of the final stage without crossing 50 Ω. This will simplify the total line–up layout and save space and components. Figures 18 to 20 show the circuit diagram and the layout of the amplifier. Figures 21 and 22 show the results obtained versus frequency.



C1, C3	8.2 pF (AVX ACCUP)	C10	2.2 pF (AVX ACCUP)
C2	18 pF (AVX ACCUP)	C11, C12, C13, C14	470 pF (NPO)
C4, C6, C7, C8	10 pF (AVX ACCUP)	R1, R3	3.9 kΩ
C5	12 pF (AVX ACCUP)	R2, R4	1 kΩ
C9	2.7 pF (AVX ACCUP)	R5	15 Ω

Figure 18. Two-Stage Electrical Schematic

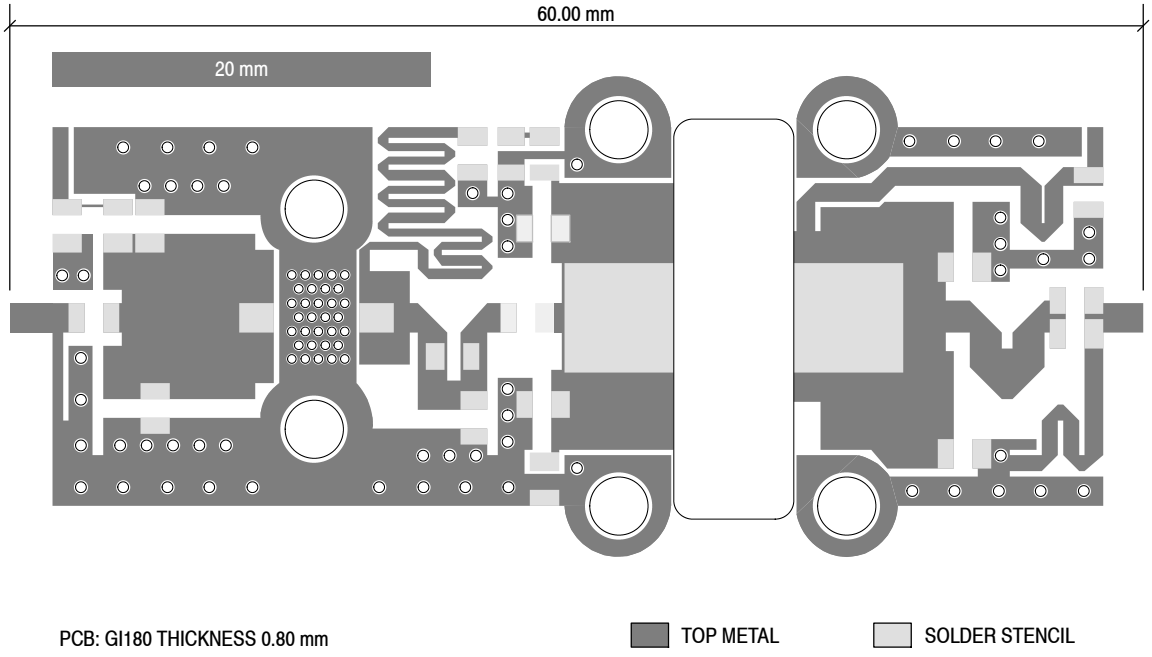


Figure 19. Two-Stage PCB

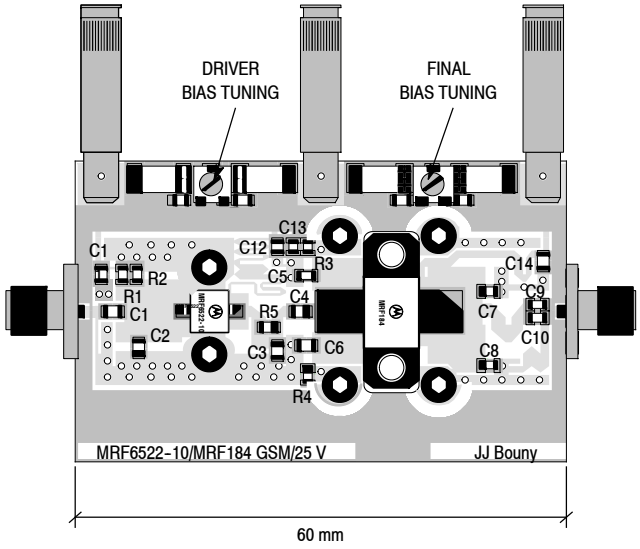


Figure 20. Two-Stage Complete Amplifier

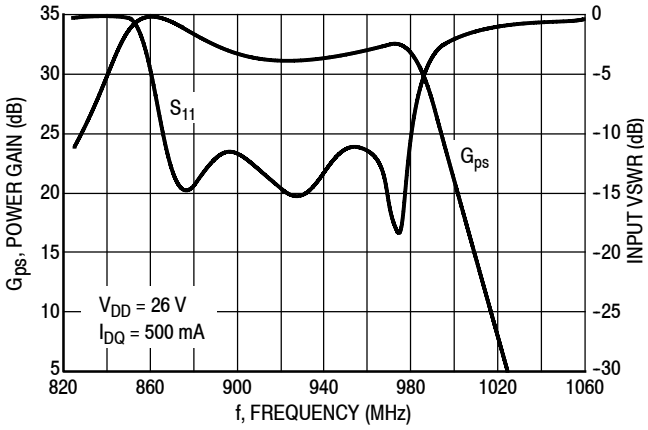


Figure 21. Power Gain, S_{11} = f (Frequency)

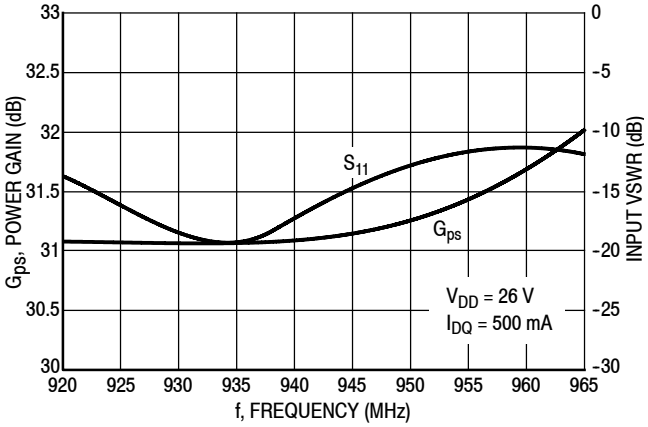


Figure 22. Power Gain, S_{11} = f (Frequency)

At 1 dB compression, the following results are obtained:

925 MHz / 26 V / 35°C base-plate
65 W / **30.0 dB** gain / **53.3%** efficiency

960 MHz / 26 V / 35°C base-plate
63 W / **30.4 dB** gain / **51.4%** efficiency

It can be seen that the performances of the two-stage amplifier are similar to those obtained for the final stage alone. This is because the driver has been a little bit oversized, and it does not bring any gain compression on the total line-up. This increases the power capability of the complete amplifier and also increases the overall efficiency.

MANUFACTURABILITY ANALYSIS

In order to verify the potential reliability and manufacturability of the design, a risk analysis (placement of the components and of the RF transistor) and thermal measurements have been done on the two-stage amplifier. Thermal measurements have been done with an infrared microscope (Computherm III from Barnes), and provide the picture in Figure 23 where one can see the temperature of the different matching elements. The amplifier was on a heat sink and temperature was regulated to obtain 70°C at the temperature test point (in the brass base plate).

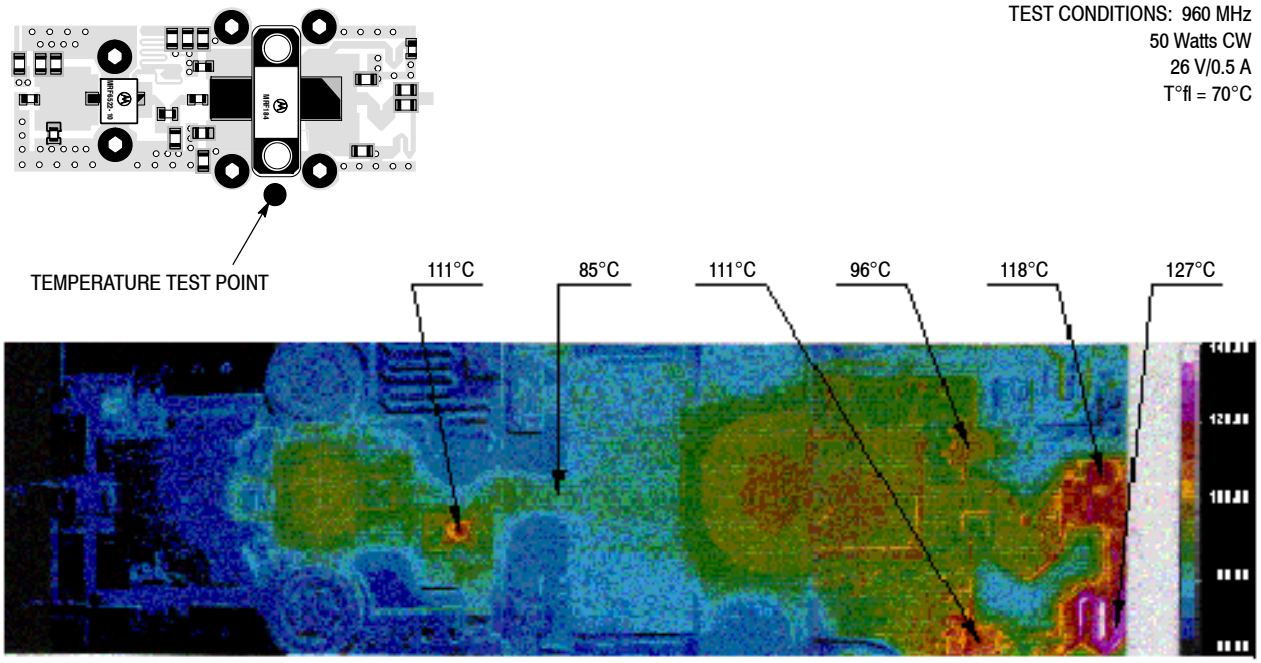


Figure 23. Two-Stage IR Scanning

The risk analysis has been done on the positioning of the input and output capacitors and on the positioning of the RF transistor. Capacitors were moved by ±0.1 mm on each side (window within the solder mask), and the RF transistor was moved by ±0.2 mm within the groove in the drain-gate axis. Results given below show extreme variations of power, efficiency and gain.

Input Matching:

P_{out} @ 1 dB (W)	Eff @ 1 dB (%)	G_{ps} @ 1 dB (dB)
± 0.5	±1	±0.15

Output Matching:

P_{out} @ 1 dB (W)	Eff @ 1 dB (%)	G_{ps} @ 1 dB (dB)
± 0.65	±0.6	±0.2

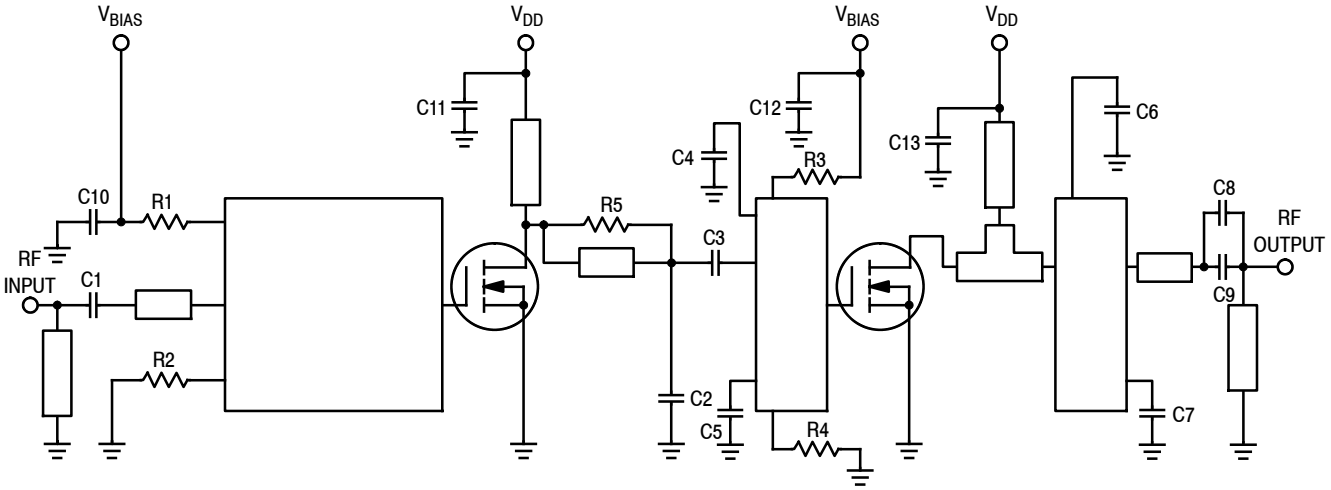
Device Positioning:

P_{out} @ 1 dB (W)	Eff @ 1 dB (%)	G_{ps} @ 1 dB (dB)
± 0.5	±1	±0.1

Bad grounding of the PCB near the transistor also has been simulated without significative effect.

ALTERNATIVE DESIGN

There are many ways to optimize the performance of an RF amplifier. One way would be to select a PCB material with improved thermal properties, such as a 0.51 mm thick RO4003 from ROGERS, and solder it down to a thin metal base plate. When making these changes, as described in Figures 24 and 25, the temperature of the matching elements is significatively reduced; the output parallel line goes from 127°C down to 98°C, and the maximum temperature of capacitors C8 and C9 goes from 118°C down to 85°C with 70°C at the temperature test point.



	MRF6522-10		MRF184
C1	8.2 pF (AVX ACCUP)	C9	2.7 pF (AVX ACCUP)
C2	10 pF (AVX ACCUP)	C10, C11, C12, C13	470 pF (NPO)
C3	8.2 pF (AVX ACCUP)	R1, R3	3.9 kΩ
C4, C5, C6, C7	10 pF (AVX ACCUP)	R2, R4	1 kΩ
C8	3.3 pF (AVX ACCUP)	R5	22 Ω

Figure 24. Alternative Two-Stage Electrical Schematic

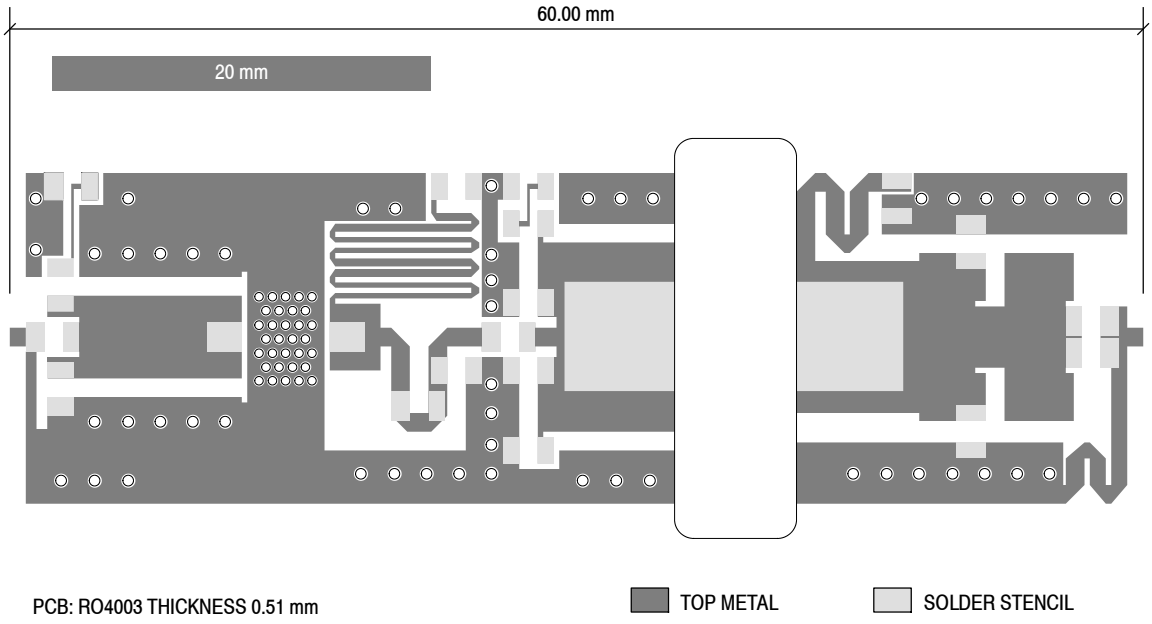


Figure 25. Alternative Two-Stage PCB

CONCLUSION

It has been shown that it was possible to build a simple compact amplifier for GSM 900 MHz base stations by using only two stages of Freescale LDMOS transistors. Performances are good even on an epoxy substrate (more than 60 W, 30 dB gain and 50% total efficiency). The design can be easily reproduced for the driver or final stage only, or for the two-stage amplifier. Two solutions are proposed using two types of PCB material, with two ways of mounting the PCB. The choice between these solutions will depend on the actual design rules used for the design of the radio, as well as the manufacturing capabilities. A complete set of measurements shows that this application is well suited for the GSM specification.

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