ANALOG DEVICES

APPLICATION NOTE

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Achieving phase coherence between multiple Fractional-N PLLs ADF4350 Phase Resync and Phase Programmability

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Introduction

Phase coherence is defined as the state in which two signals maintain a fixed phase relationship between each other and is typically required for evaluating the performance of phased-array antennas as well as for test and measurement equipment.

For integer-N PLLs, it is relatively straightforward to achieve phase coherence between multiple PLLs by using the same reference for each PLL and updating each device at the same time to ensure the PLL counters are aligned. This is often achieved by updating the PLL register contents with the new frequency word while holding the device in reset. To ensure both parts get updated at the same time, the reset signal is made common and so is cleared internally in the PLLs at exactly the same time. This ensures the internal dividers in the PLL start counting from the same start-point. See here for a good reference on achieving integer-N PLL phase coherence using this method. If the output frequencies on both parts are updated at the same time then the consistent output phase will be maintained between the multiple PLLs. To achieve absolute phase consistency with respect to the reference input requires you to update the PLLs at a rate equal to an integer multiple of N-divide (PLL feedback divider) times REFIN cycles. This would mean the reset signal would need to be synchronized with the reference and a count done internally in a microcontroller to keep synchronization. In many cases the absolute phase consistency is not required just that the relative phase between the PLL outputs is kept constant. In this case LE can be asynchronous to the reference input.

For a fractional-N PLL however, the output can settle to any one of MOD phase offsets with respect to the input reference, where MOD is the fractional modulus. If you are comparing multiple frac-N PLL outputs you will not achieve relative phase coherence between the PLLs as in the integer-N PLL case. Applying a simple reset signal like in the integer-N case is not sufficient for the fractional-N PLL because any cycle slips that could occur during the frequency settling transient could potentially upset the relative phase relationship. The solution to this is to apply the reset signal after the frequency transient to avoid any cycle slip events. See here for explanation on PLL cycle slipping.

This reset would have to be applied after each and every frequency settling transient (i.e. when you update the frequency) as a cycle slip could potentially have occurred during the transient. The frac-N

PLL count sequence repeats every MOD cycles so the reset needs to occur at an integer multiple of MOD x REFIN cycles to keep the same absolute output phase on a given output frequency.

Luckily both of these reset requirements are taken care of internally in the ADF4350 by means of the phase resync feature. In addition to this document the user should also refer to the Phase Resync section in the datasheet for details on programming a specific RF output phase when using phase resync.

Setup

The setup to measure the phase difference between two identical ADF4350 evaluation boards is shown in Figure 1. Phase difference is measured using the AD8302 phase detector. Alternatively you could measure relative phase using a Vector Network analyser.

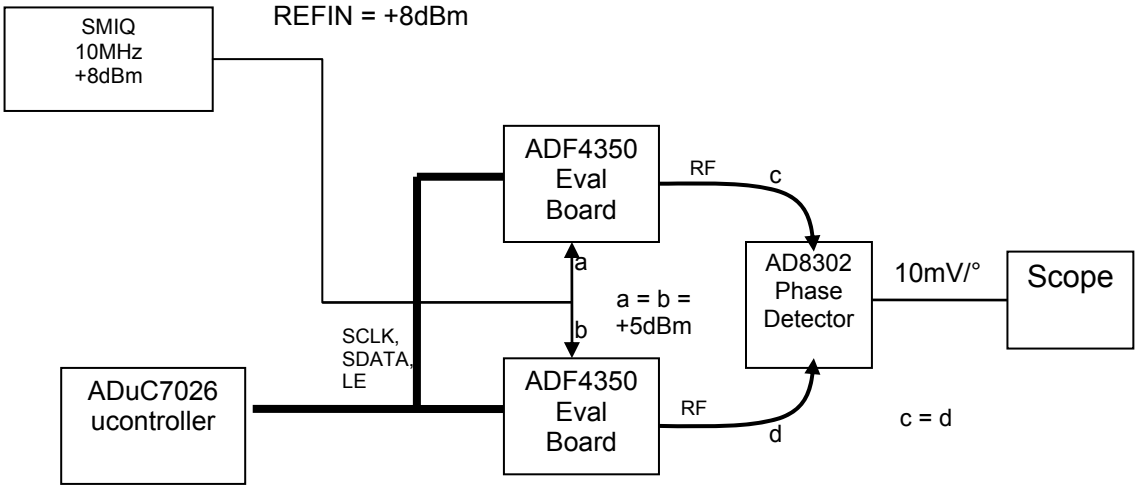

Figure 1.

To ensure the ADF4350 PLL does not get updated during a counter reset period which could upset the output phase, it is recommended to synchronise the LE signal to the rising edge of REFIN. This can be done using an external flip-flop. The setup in Figure 1 uses a flip-flop in a Programmable Logic array in the ADuC7026 microcontroller. A simpler setup which can be used to see the basic operation of the phase resync is shown in the Appendix. This can be used to test the initialisation loop described later.

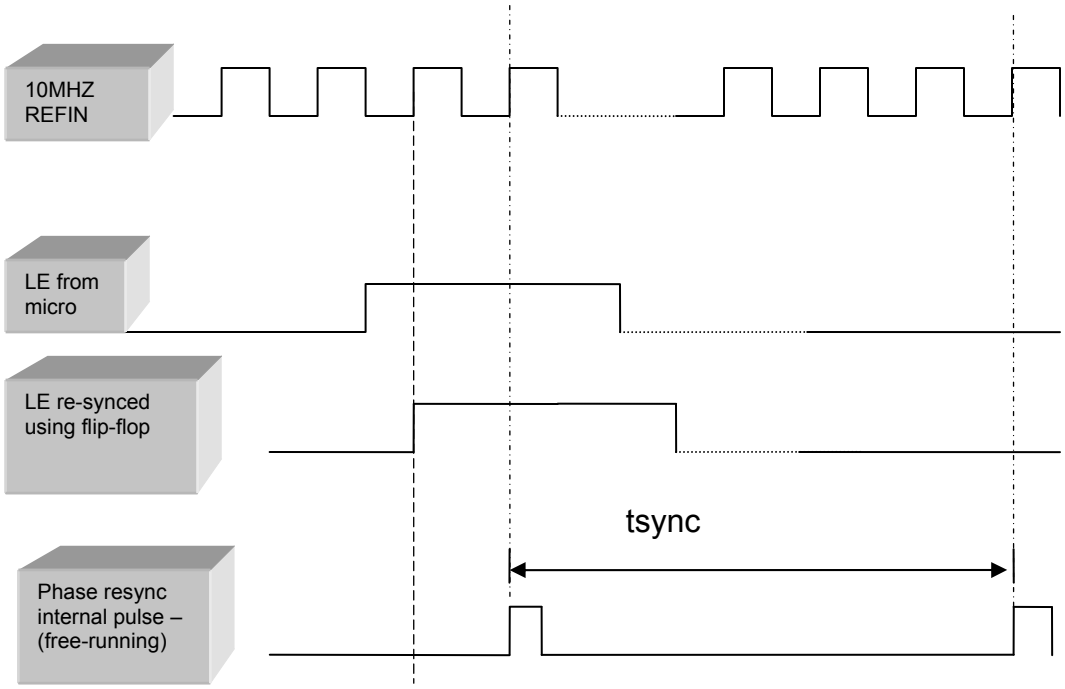

Figure 2.

Equal length of cables and symmetry in load on LE and REFIN lines

It is important that the split REFIN signal is connected to both ADF4350s using equal cable lengths. Probing the REFIN signal using a 15pF scope probe has the effect of skewing the REFIN edge. If it is required to monitor REFIN on one ADF4350, then make sure the other board is equally loaded. Equal length cables should also be used to connect the two RF outputs to the AD8302 phase detector as any mismatch will cause a phase offset and thus an offset in the AD8302 output voltage. The AD8302 output voltage is in the range 0 to ~1.8V, corresponding to 0 to 180 degrees. It's linear in degrees, scaled 10mV/° between ~20 to ~160 degrees.

PLL loop filter

The PLL loop filters of both ADF4350 should also be the same to ensure close as possible symmetry in phase settling transients.

Pin-mapping on ADuC7026 EVB for ADF4350 timing experiments

Example Code for the ADuC7026 is available on request from Analog Devices to perform both the LE synchronization and the SPI write function. The pin-mapping used is as follows:

From ADuC7026	To ADF4350 EVB	
P1.4 (SCLK)	T4 (CLK)	
P1.6 (MOSI)	T5 (DATA)	
P1.5 (MISO)	NC	No Connect
P2.0 (unsynchronized LE out)		Connect P2.0 to P3.0 (PLAIN) on micro EVB
P4.0 (synchronized LE out)	T6 (LE)	PLAOUT
P2.1 (scope trigger signal)		trigger signal for oscilloscope when performing hopping test.
P0.7 (10MHz_sync input)		clock input for PLA, connect 10MHz function generator output to P0.7
GND	GND	Ensure boards share a common Ground

Table 1. ADuC7026 to ADF4350 pin-mapping

ADF4350 Settings needed for phase coherence

1. Feedback select set to feedback divider output to N-Counter rather than the VCO signal directly(R4:DB23 = 0)
2. Use phase resync feature ensuring tsync > 400us
3. Refin to LE alignment (synchronise LE to positive edge of REFIN)
4. Make sure you are in fractional mode. Phase resync does not work in integer mode
5. Make sure all ADF4350s use same loop filter components and charge pump settings.

Results

The AD8302 phase output was captured on a scope in infinite persistence mode for the following setups:

1. Initialisation loop – re-write initialisation sequence every 60ms
2. Frequency Hopping, channel hop from 2.4001GHz to 1.2001GHz
3. Phase adjustment sweep, adjust phase from 1 to 18
4. Power-down loop

1. Initialisation Loop

Using the setup as described in Figure 1 an initialisation sweep was performed where the same initialisation sequence with phase resync enabled was re-written to both parts every 25ms in a loop. The initialisation loop consisted of 6 register writes from Register 5 to Register 0 in descending order. After the Register 0 write a VCO calibration is initiated to select the correct VCO band even though in this case we are programming the same frequency. The output phase difference between the two ADF4350 outputs was monitored by probing the Phase output pin (V_{PHS}) of the AD8302 on an oscilloscope. The AD8302 phase output voltage vs. input phase difference transfer function is as shown in Figure 4 and has approx. a 10mV/deg slope. So for phase coherence between the two ADF4350 outputs you would need the AD8302 phase out to be a constant voltage. The measured AD8302 phase out during the initialisation loop (scope in infinite persistence mode) is shown in Figure 3 and is triggered off the final Register 0 write.The phase difference between the two ADF4350s is indeterminate during the VCO calibration period as the PLL is kept open-loop. After the VCO calibration is complete the phase resync is enabled which products a constant output voltage on the AD8302 output and hence a coherent phase between the two ADF4350s.

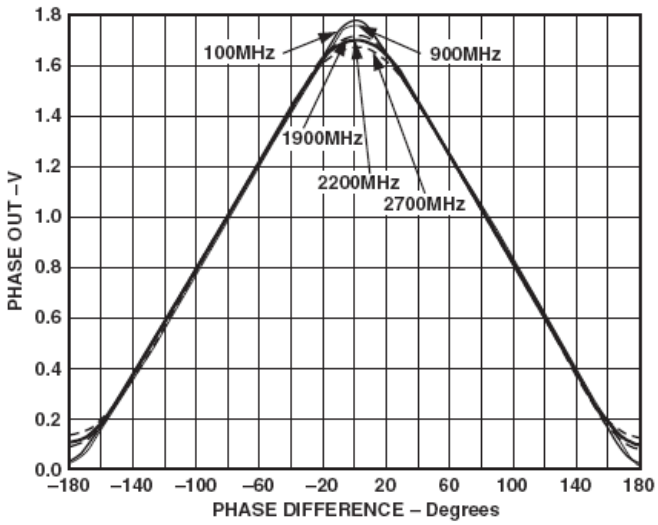

Figure 3. Phase Output (VPHS) vs. Input Phase Difference, Input Levels –30 dBm,

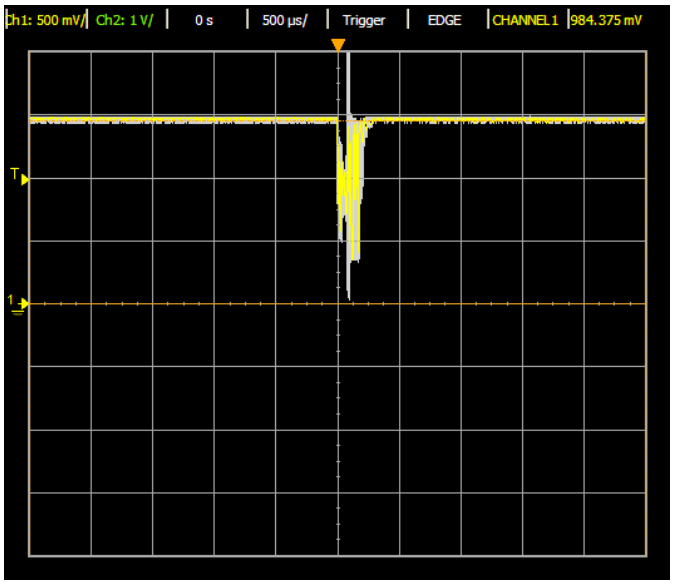

Figure 4. Phase Output (VPHS) of AD8302 while ADF4350 written to in constant initialization loop (R4:DB23) =0

As an experiment the feedback to the PLL was chosen as the fundamental signal rather than the divided output (this does not meet the requirements listed under ADF4350 Settings needed for phase coherence). The AD8302 output in this case is shown in Figure 5. which shows 4 distinct output phase values. This is because the RF dividers (div-by-4 in this case) are not sycnronised across multiple ADF4350s and so could settle to any of 4 distinct output divider phases. In this case phase coherence is not maintained.

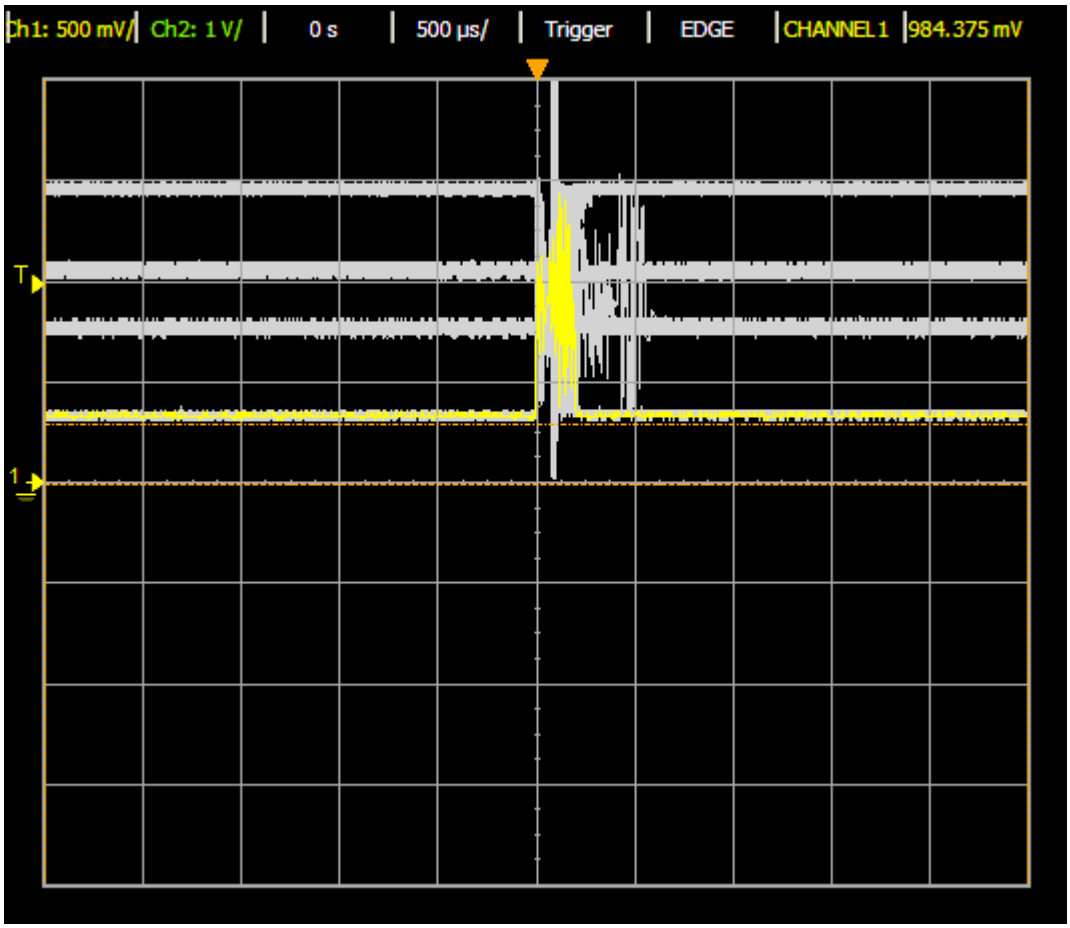

Figure 5. Phase Output (VPHS) of AD8302 while ADF4350 written to in constant initialization loop. (R4:DB23) =1

2. Frequency Hopping Sweep

Using the same setup as described in Figure 1 a frequency hopping sweep was performed to show consistent phase on a given channel, when two ADF4350s are programmed to jump to a new frequency and then return to the original frequency. In this case the ADF4350s were programmed to hop between 2.4001GHz to 1.2001GHz. The scope trigger was set to trigger at the start of each 2.4GHz to 1.2GHz jump to monitor the frequency and phase transients. The frequency transient was viewed by probing the Vtune input pin to the ADF4350. The phase transient was monitored as before on the AD8302 V_{PHS} output.

The MOD value was set to 18 which gives 18 possible RF output phases the PLL could settle to after each frequency update. The AD8302 phase detector is linear over a 180 degree range, i.e. it can't discriminate between + 100deg and -100degrees. This means the AD8302 V_{PHS} output should display MOD/2 or 9 distinct phase output values after the initial PLL settling, which is shown in Figure 6. The scope display was set to infinite persistence mode to capture the different phase settling transients.

Figure 6 also shows the action of the phase resync function which causes the AD8302 output to settle to a consistent phase after the timeout period set by t_{sync} which was programmed to be:

tsync = 300 x 18 x 1/10MHz

= 540us

A constant voltage at the output of the AD8302 phase detector implies a constant phase difference between the two RF inputs (two ADF4350 devices), this phase coherence is achieved even during frequency hopping.

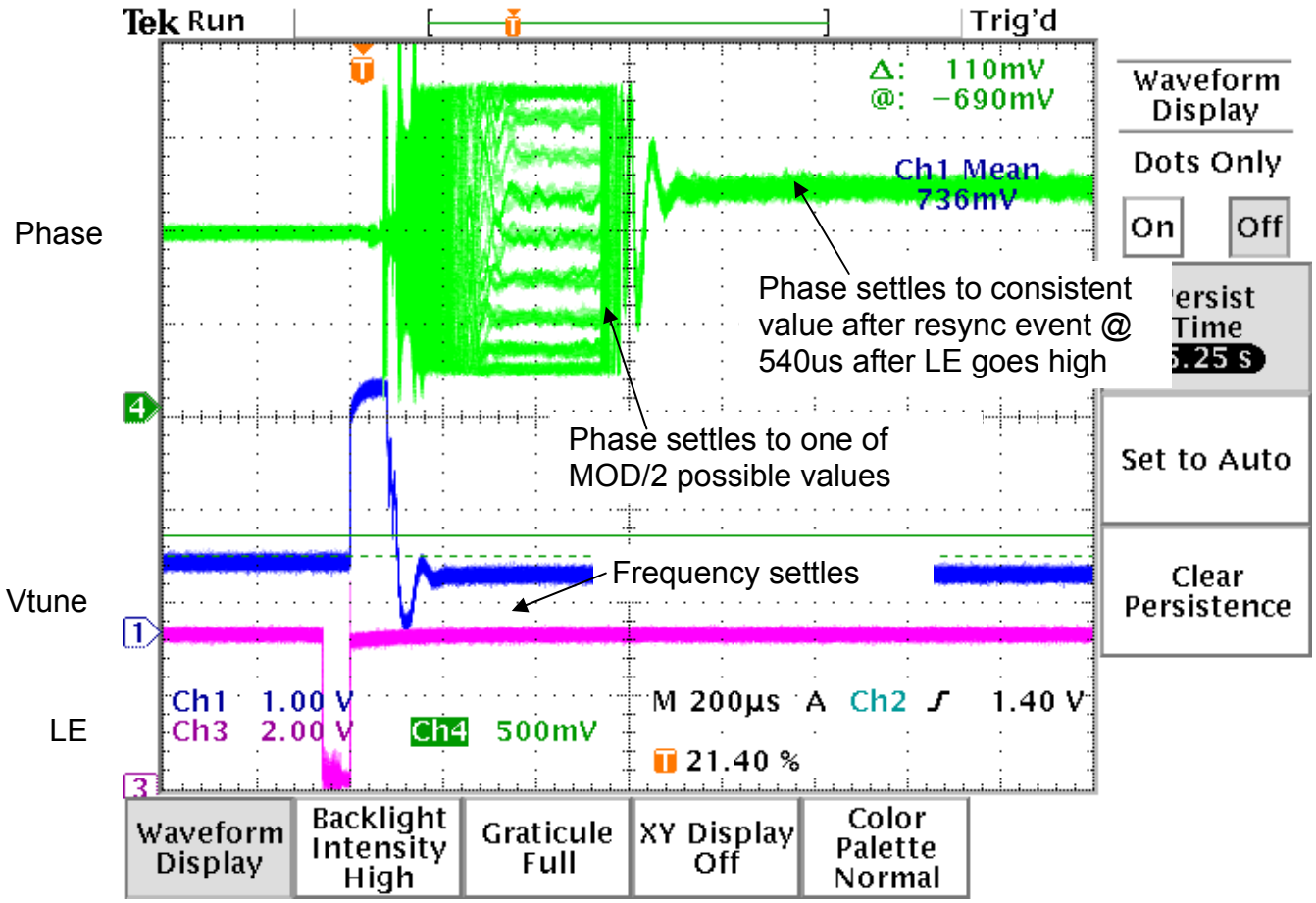

Figure 6. Frequency hopping. T_{SYNC} programmed to be 300 x 18 x 1/10MHz = 540us

3. Phase Adjustment Sweep

Using the same setup a phase adjustment sweep was run, where the phase value of one ADF4350 device was swept in a loop while the other ADF4350 device was kept constant to serve as the reference. The MOD value was again set to 18 with phase resync enabled and t_{sync} equal to 540us as before. The phase value which is programmed in Register 1 was swept on one

ADF4350 device from 1 to 18 to cover a full 360 degrees phase sweep. Setting the MOD equal to 18, means each phase value increment corresponds to a phase increment of :

$\Phi = 360/MOD = 360/18 = 20deg$

which gives a voltage increment at the AD8203 phase output of:

20deg x 10mV/deg = 200mV

The phase adjustment sweep shown in Figure 7. Each phase word increment gave approximately a 200mV voltage change at the AD8302 V_{PHS} output as expected. Because the AD8302 is only linear over 180 degrees the phase sweep wraps around after 180^{o} and so is a sinusoid rather than a saw-tooth linear over 360 degrees as you might expect. This shows the output phase control possible using the phase resync in conjunction with the phase control word in Register 1.

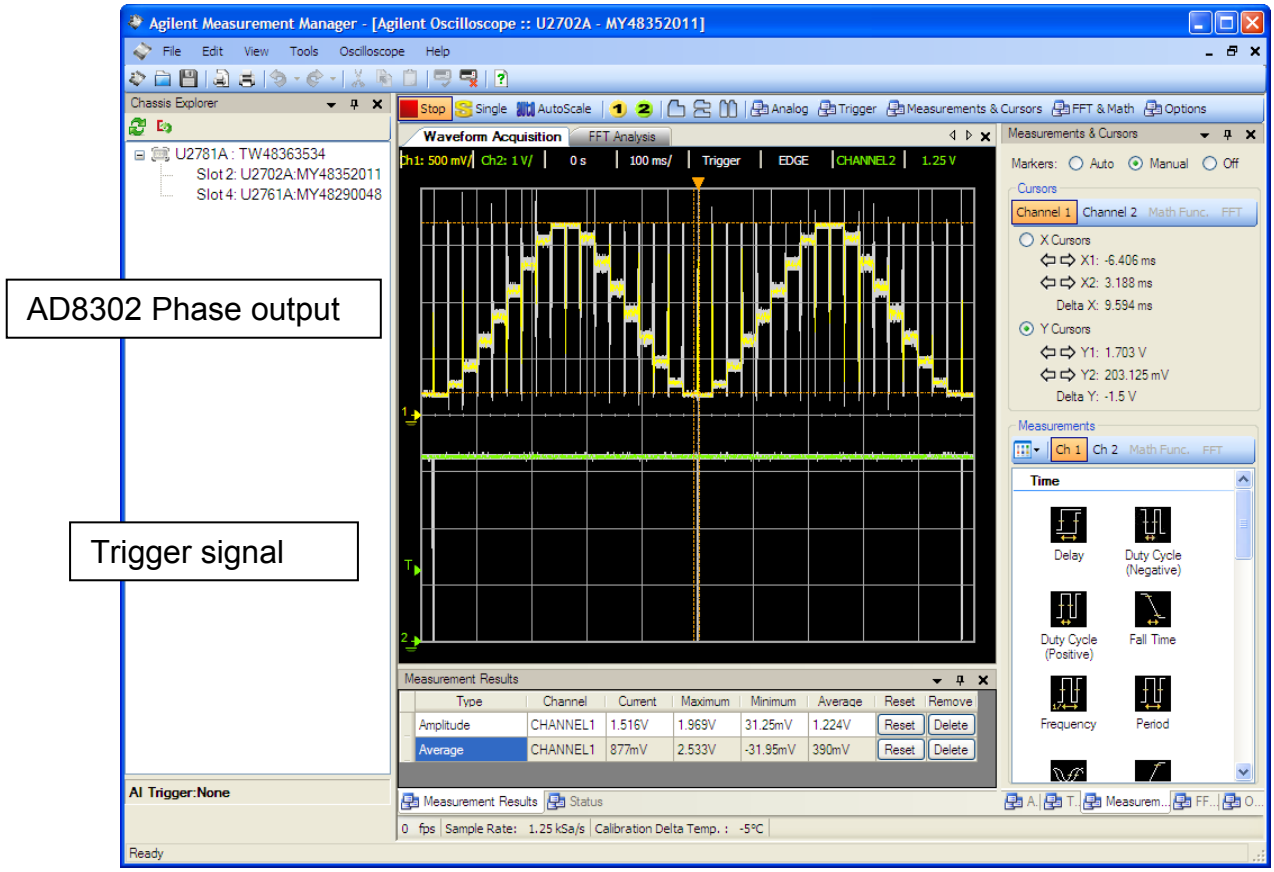

Figure 7. Phase adjustment sweep. Scope in infinite persistence mode

4. Applying Phase Resync after coming out of powerdown

When the ADF4350 is brought into powerdown mode, the VCO, RF dividers, reference circuit and phase resync counter are all powered down. To achieve phase consistency after coming out of powerdown you need to:

- Write to Register 0 twice after clearing the powerdown bit to re-enable phase re-sync. All other register contents loaded in prior to the powerdown event are kept in the internal shift register.
- After coming out of powerdown, the ADF4350 will settle on an arbitrary phase (MOD possible values). However if two or more ADF4350's with the same reference are brought out of powerdown at the same time, then these should have the same phase. This should allow a more simple calibration to remove initial phase offset on power-up.

Appendix

Simpler setup to view phase resync feature. Note if your scope is high speed enough you can omit the AD8302 and view the RF outputs and the phase relationship between the two directly.