

2SK125

www.DataSheet4U.com

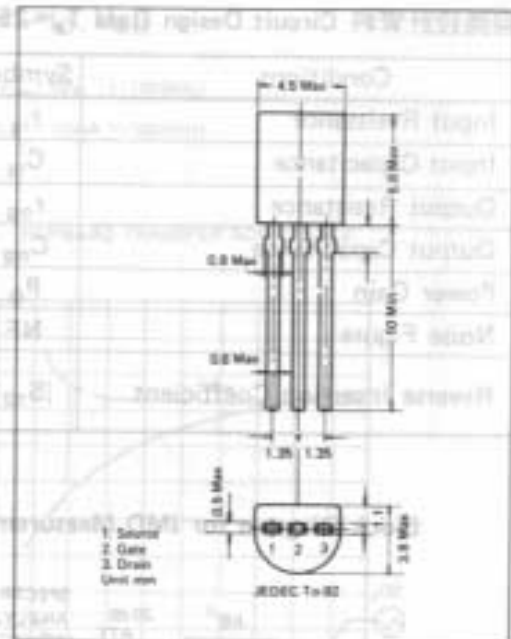
2SK125

Silicon N-Channel Junction FET

- UHF Amplifiers, Mixers (Common Gate)
- P_G : 12.5 dB Typ. ($f = 100$ MHz, Common Gate)
- NF: 1.5 dB Typ. ($f = 100$ MHz, Common Gate)
- 3rd Harmonic Distortion -52 dB Typ.
- Analogue Switchings (R_{ON} : 40 Ω Typ.)

絶対最大定格 Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Characteristics	Symbol	2SK125
Drain-to-Gate Voltage	V_{DGG}	25 V
Source-to-Gate Voltage	V_{SGG}	25 V
Drain Current	I_D	100 mA
Gate Current	I_G	10 mA
Channel Power Dissipation	P_{ch}	500 mW
Channel Temperature	T_{ch}	120 $^\circ\text{C}$
Storage Temperature	T_{stg}	-50~+120 $^\circ\text{C}$



電気的特性 Electrical Characteristics $T_A = 25^\circ\text{C}$

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gate Cutoff Current	I_{GSS}	$V_{GS} = -15\text{V}$, $V_{DS} = 0$			-10	nA
Gate-to-Source Voltage	V_{GSS}	$I_G = -10\mu\text{A}$, $V_{DS} = 0$	-25			V
Drain Saturation Current	I_{DSS}	$V_{DS} = 10\text{V}$, $V_{GS} = 0$, $PW = 300\mu\text{s}$	30		75	mA
Pinch-off Voltage	V_p	$V_{DS} = 10\text{V}$, $I_D = 100\mu\text{A}$	-2		-6	V
Forward Transfer Conductance	g_m	$V_{DS} = 10\text{V}$, $I_D = 10\text{mA}$, $f = 1\text{kHz}$	10	14		$\text{m}\Omega$
Reverse Transfer Capacitance	C_{rss}	$V_{DG} = 10\text{V}$, $I_S = 0$, $f = 1\text{MHz}$		2.6	3	pF
Power Gain	P_G	$V_{DG} = 10\text{V}$, $I_D = 10\text{mA}$, $f = 100\text{MHz}$, $BW = 2.8\text{MHz}$	10	12.5		dB
Noise Figure	NF	$V_{DG} = 10\text{V}$, $I_D = 10\text{mA}$, $f = 100\text{MHz}$, $BW = 2.8\text{MHz}$ 2nd Stage NF = 4.2 dB		1.8	2.5	dB
Intermodulation Distortion	IMD	$V_{DG} = 10\text{V}$, $I_D = 10\text{mA}$, $f_1 = 100\text{MHz}$, $f_2 = 100.1\text{MHz}$, $e_1 = 100\text{dB}\mu$	-45	-52		dB
Junction-to-Ambient Thermal Resistance	θ_{j-a}				190	$^\circ\text{C/W}$

2SK125

2SK125

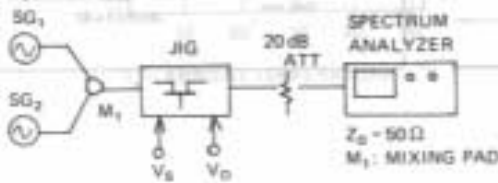
Silicon N-Channel Junction FET

回路設計資料 Circuit Design Data $T_a = 25^\circ\text{C}$

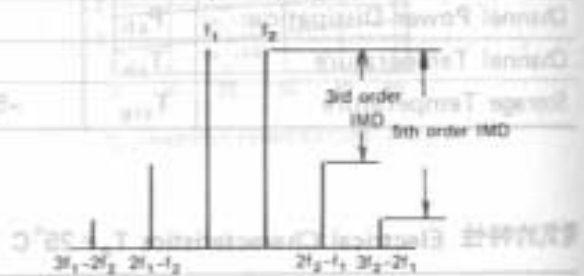
* VHF Amplifier, Mixer (Common Gate)

Conditions	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Resistance	r_{ig}	$V_{DG} = 10\text{V}, I_D = 10\text{mA},$ $f = 100\text{MHz}$		70		Ω
Input Capacitance	C_{ig}			3.0		pF
Output Resistance	r_{og}			5		$k\Omega$
Output Capacitance	C_{og}			3.0		pF
Power Gain	P_G	$V_{DG} = 10\text{V}, I_D = 10\text{mA},$ $f = 500\text{MHz}, \text{BW} \approx 12\text{MHz}$		7.0		dB
Noise Figure	NF				4.0	dB
Reverse Insertion Coefficient	$ S_{12} $	$V_{DG} = 10\text{V}, I_D = 10\text{mA},$ $f = 500\text{MHz}$		0.035		

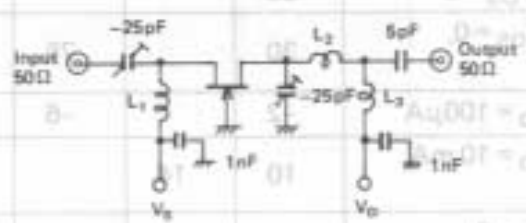
Block Diagram for IMD Measurement



Frequency Spectrum



P_G & NF Test Circuit ($f = 100\text{MHz}$)



IMD Test Circuit ($f = 100\text{MHz}$)

